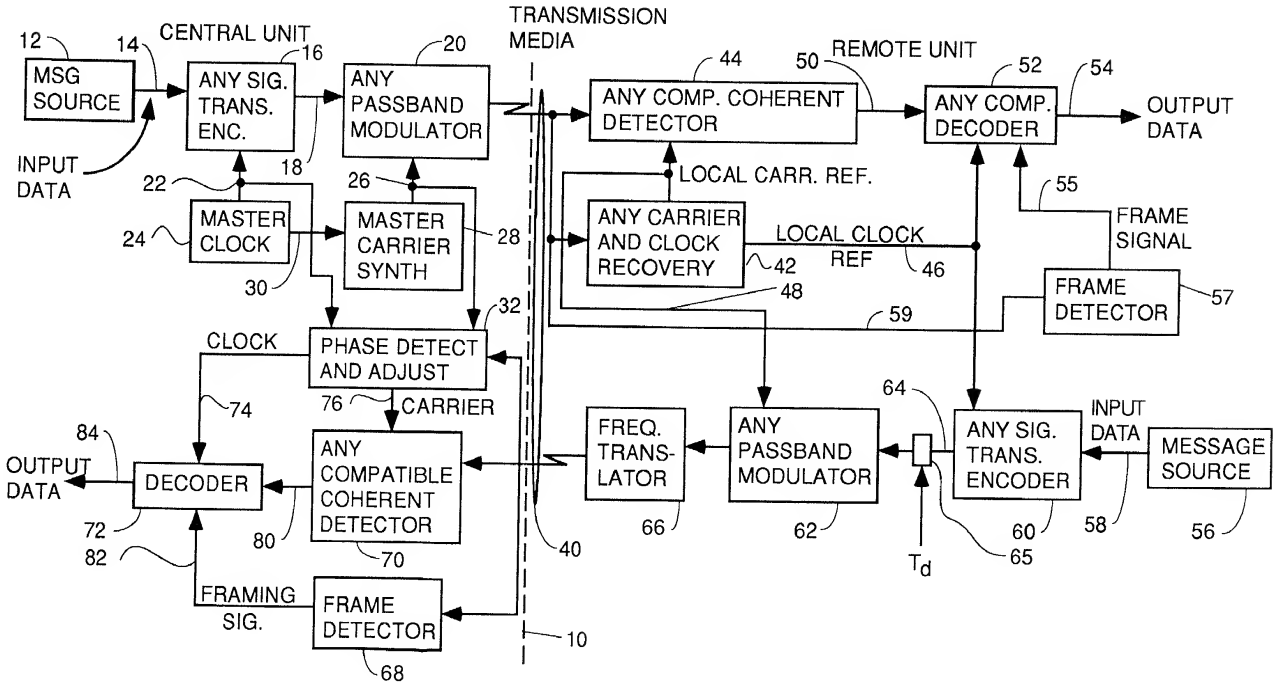

12
MSG SOURCE
14
CENTRAL UNIT
ANY SIG. TRANS. ENC.
16
INPUT DATA
18
20
ANY PASSBAND MODULATOR
TRANSMISSION MEDIA
22
MASTER CLOCK
24
26
MASTER CARRIER SYNTH
28
30
32
CLOCK
PHASE DETECT AND ADJUST
74
76
CARRIER
84
OUTPUT DATA
DECODER
72
82
ANY COMPATIBLE COHERENT DETECTOR
80
70
FRAMING SIG.
FRAME DETECTOR
68
10
40
44
ANY COMP. COHERENT DETECTOR
50
REMOTE UNIT
LOCAL CARR. REF.
ANY CARRIER AND CLOCK RECOVERY
42
48
LOCAL CLOCK REF
46
59
52
ANY COMP. DECODER
54
OUTPUT DATA
55
FRAME SIGNAL
FRAME DETECTOR
57
64
FREQ. TRANS-LATOR
66
ANY PASSBAND MODULATOR
62
T_d
ANY SIG. TRANS. ENCODER
60
65
INPUT DATA
58
MESSAGE SOURCE
56

FIG. 1

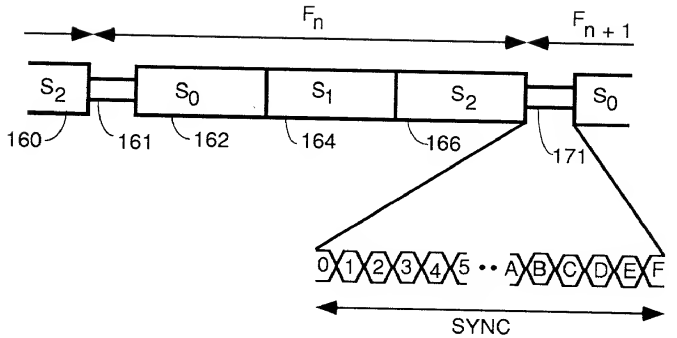

F_n
F_{n+1}
S_2
S_0
S_1
S_2
S_0
160
161
162
164
166
171
0 1 2 3 4 5 • • A B C D E F
SYNC

FIG. 2A

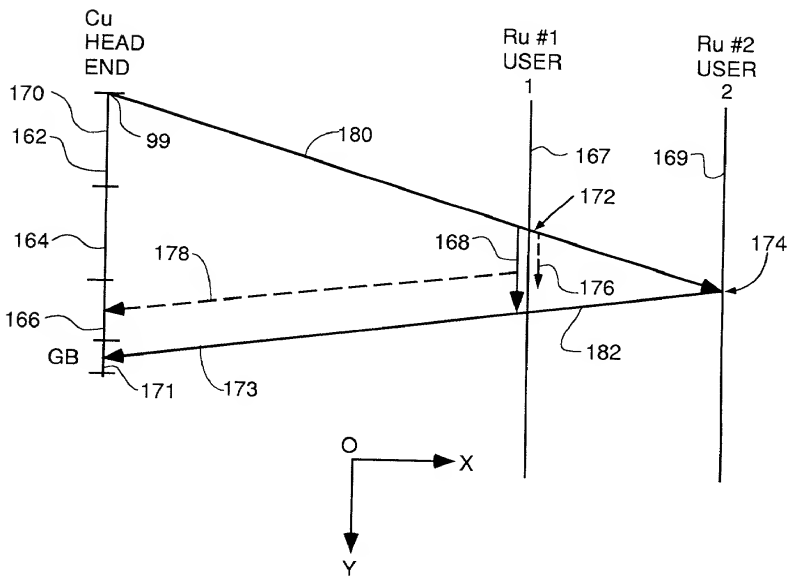
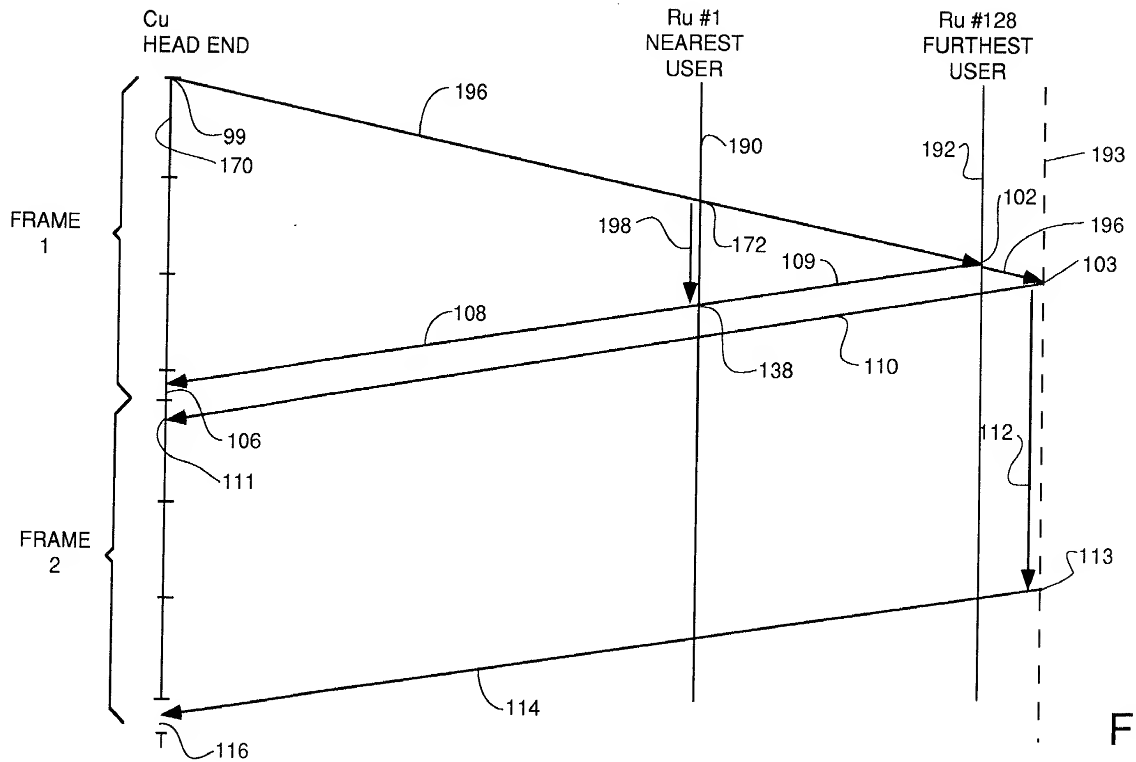

Cu
HEAD
END
Ru #1
USER
1
Ru #2
USER
2
170
162
99
180
167
169
172
164
178
168
174
176
166
GB
182
171
173
O
X
Y

FIG. 2B



Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
FRAME
1
FRAME
2
196
99
170
190
192
193
102
196
198
172
109
103
108
138
110
106
111
112
113
114
T
116

FIG. 3

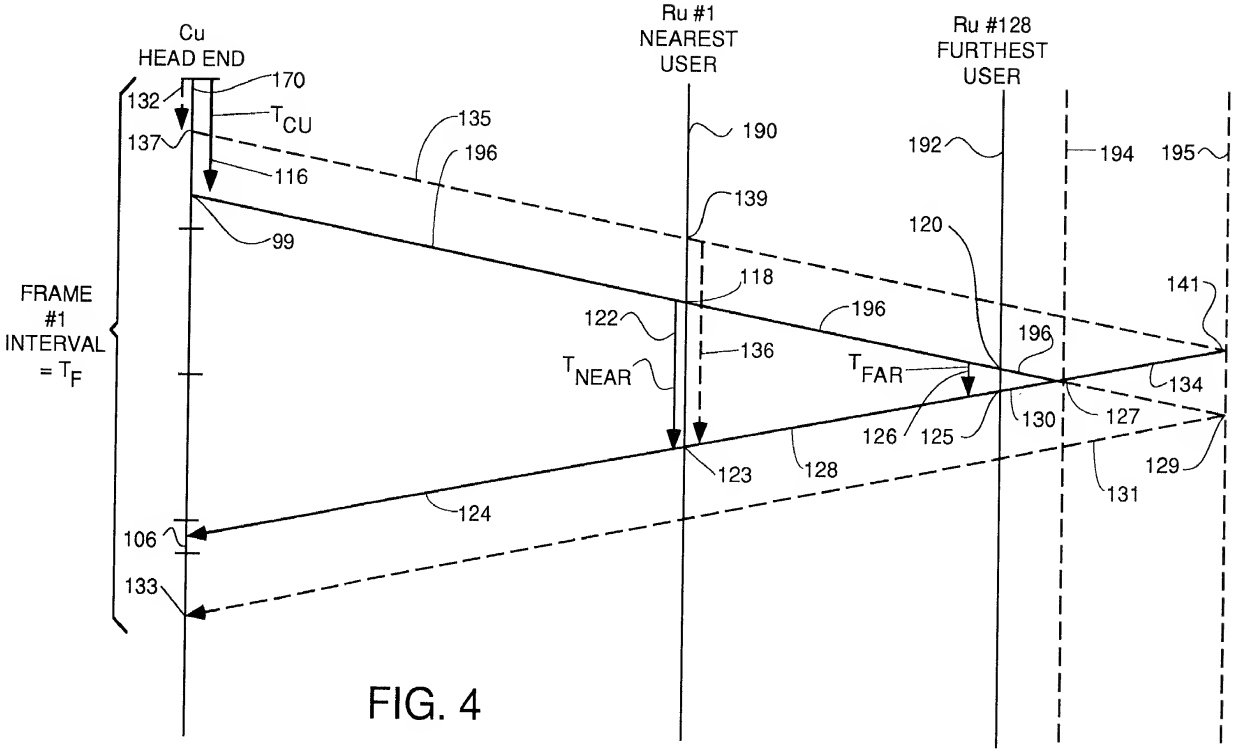
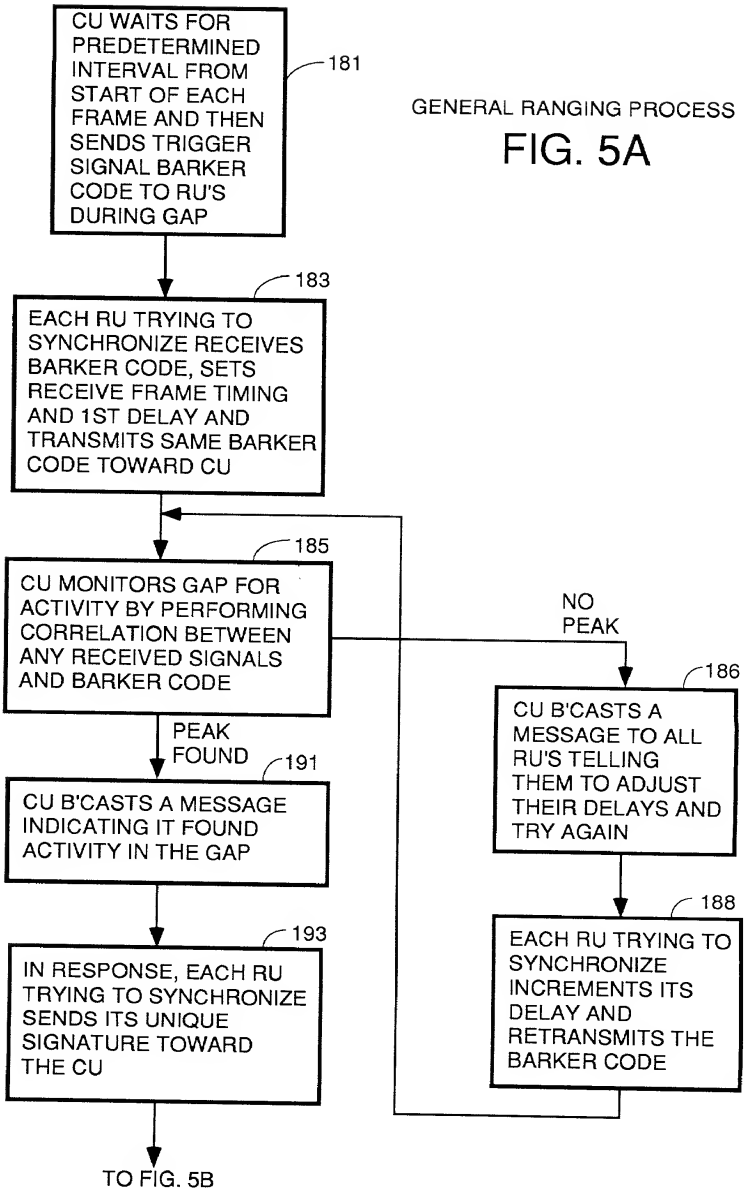


FIG. 4



GENERAL RANGING PROCESS

FIG. 5A

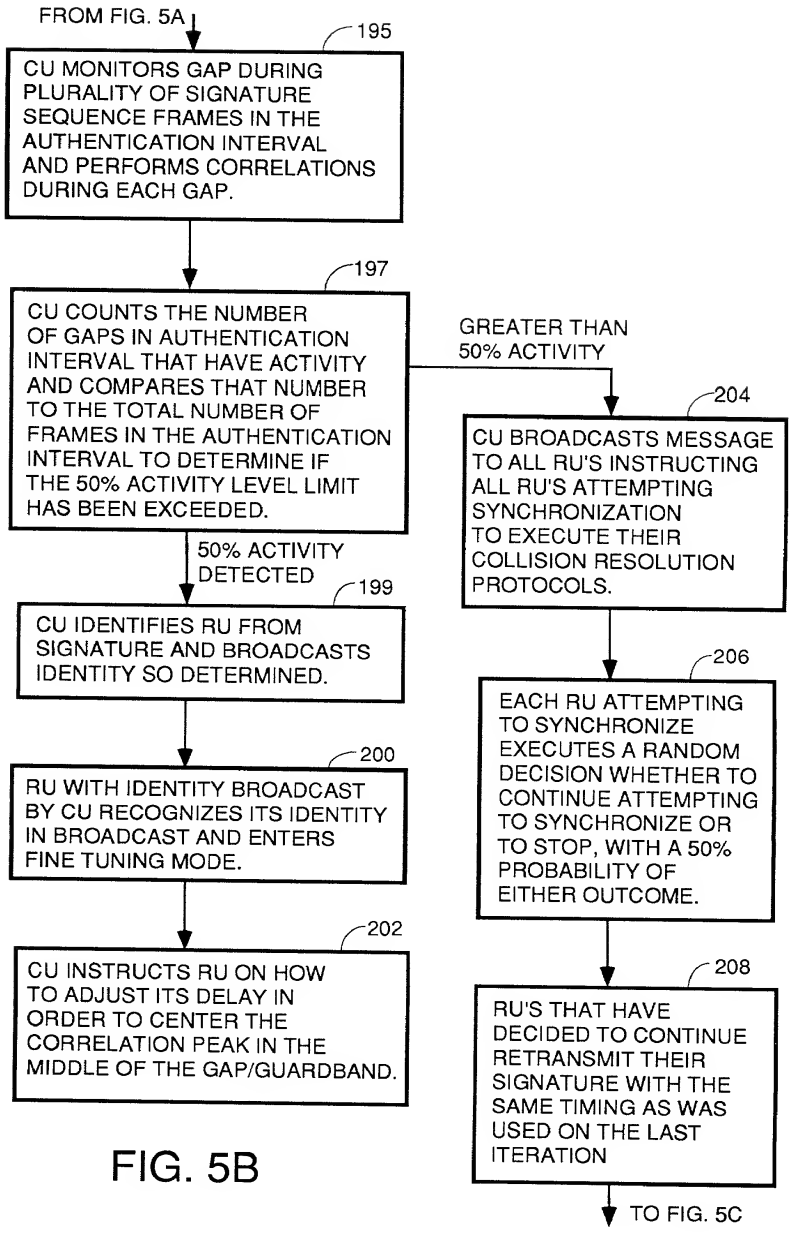

FROM FIG. 5A
195
CU MONITORS GAP DURING PLURALITY OF SIGNATURE SEQUENCE FRAMES IN THE AUTHENTICATION INTERVAL AND PERFORMS CORRELATIONS DURING EACH GAP.
197
CU COUNTS THE NUMBER OF GAPS IN AUTHENTICATION INTERVAL THAT HAVE ACTIVITY AND COMPARES THAT NUMBER TO THE TOTAL NUMBER OF FRAMES IN THE AUTHENTICATION INTERVAL TO DETERMINE IF THE 50% ACTIVITY LEVEL LIMIT HAS BEEN EXCEEDED.
50% ACTIVITY DETECTED
199
CU IDENTIFIES RU FROM SIGNATURE AND BROADCASTS IDENTITY SO DETERMINED.
200
RU WITH IDENTITY BROADCAST BY CU RECOGNIZES ITS IDENTITY IN BROADCAST AND ENTERS FINE TUNING MODE.
202
CU INSTRUCTS RU ON HOW TO ADJUST ITS DELAY IN ORDER TO CENTER THE CORRELATION PEAK IN THE MIDDLE OF THE GAP/GUARDBAND.
GREATER THAN 50% ACTIVITY
204
CU BROADCASTS MESSAGE TO ALL RU'S INSTRUCTING ALL RU'S ATTEMPTING SYNCHRONIZATION TO EXECUTE THEIR COLLISION RESOLUTION PROTOCOLS.
206
EACH RU ATTEMPTING TO SYNCHRONIZE EXECUTES A RANDOM DECISION WHETHER TO CONTINUE ATTEMPTING TO SYNCHRONIZE OR TO STOP, WITH A 50% PROBABILITY OF EITHER OUTCOME.
208
RU'S THAT HAVE DECIDED TO CONTINUE RETRANSMIT THEIR SIGNATURE WITH THE SAME TIMING AS WAS USED ON THE LAST ITERATION
TO FIG. 5C

FIG. 5B

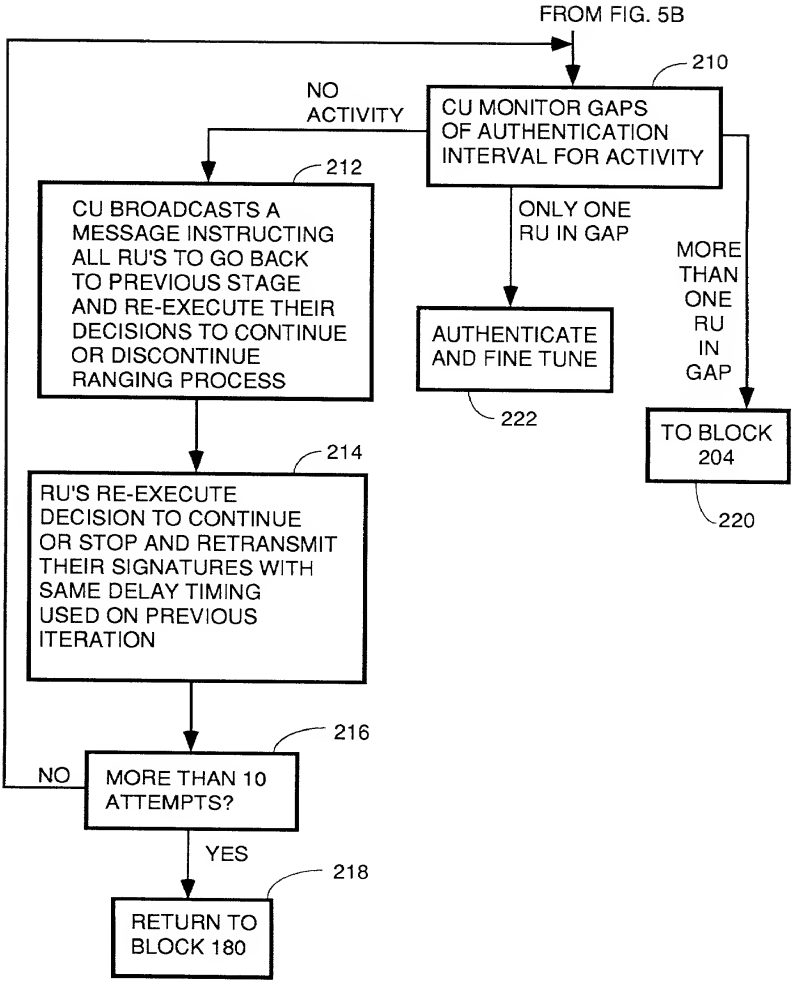

FROM FIG. 5B
210
CU MONITOR GAPS OF AUTHENTICATION INTERVAL FOR ACTIVITY
NO ACTIVITY
212
CU BROADCASTS A MESSAGE INSTRUCTING ALL RU'S TO GO BACK TO PREVIOUS STAGE AND RE-EXECUTE THEIR DECISIONS TO CONTINUE OR DISCONTINUE RANGING PROCESS
ONLY ONE RU IN GAP
AUTHENTICATE AND FINE TUNE
222
MORE THAN ONE RU IN GAP
TO BLOCK 204
220
214
RU'S RE-EXECUTE DECISION TO CONTINUE OR STOP AND RETRANSMIT THEIR SIGNATURES WITH SAME DELAY TIMING USED ON PREVIOUS ITERATION
216
NO
MORE THAN 10 ATTEMPTS?
YES
218
RETURN TO BLOCK 180

FIG. 5C

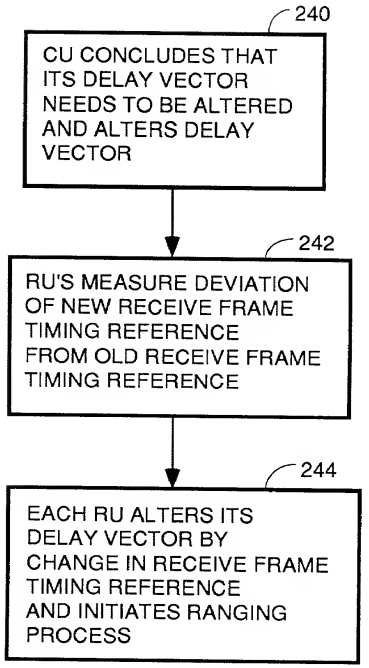


FIG. 6
DEAD RECKONING RE-SYNC

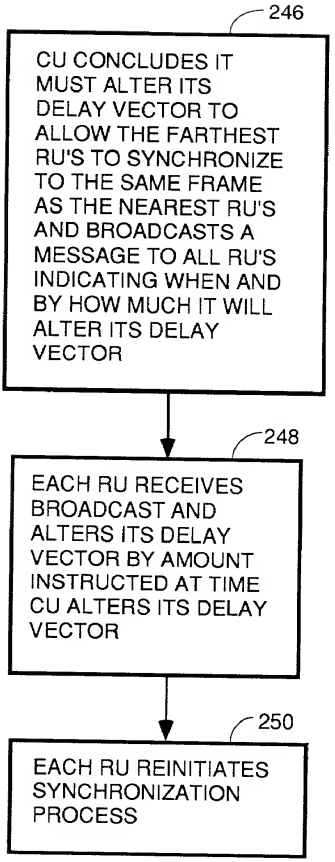
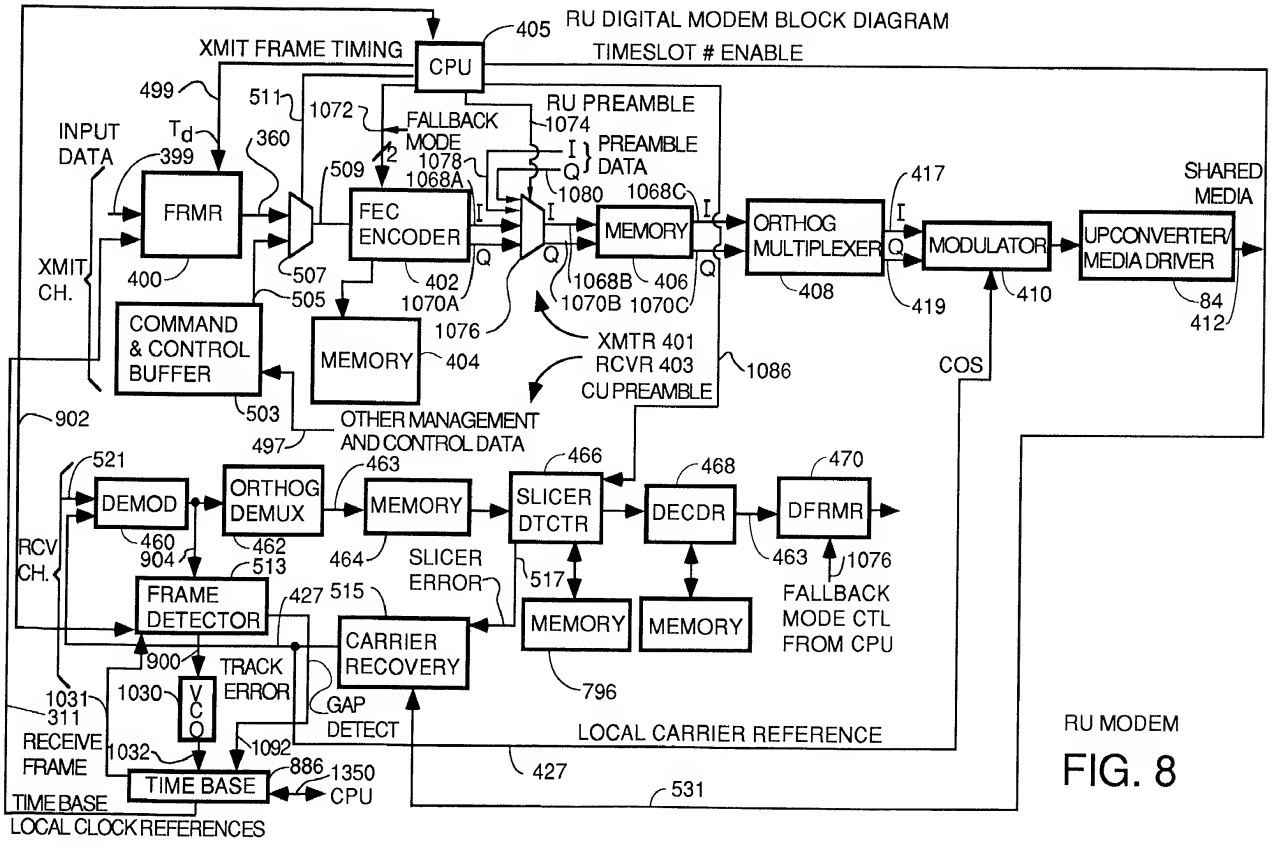


FIG. 7
PRECURSOR EMBODIMENT



RU MODEM

FIG. 8

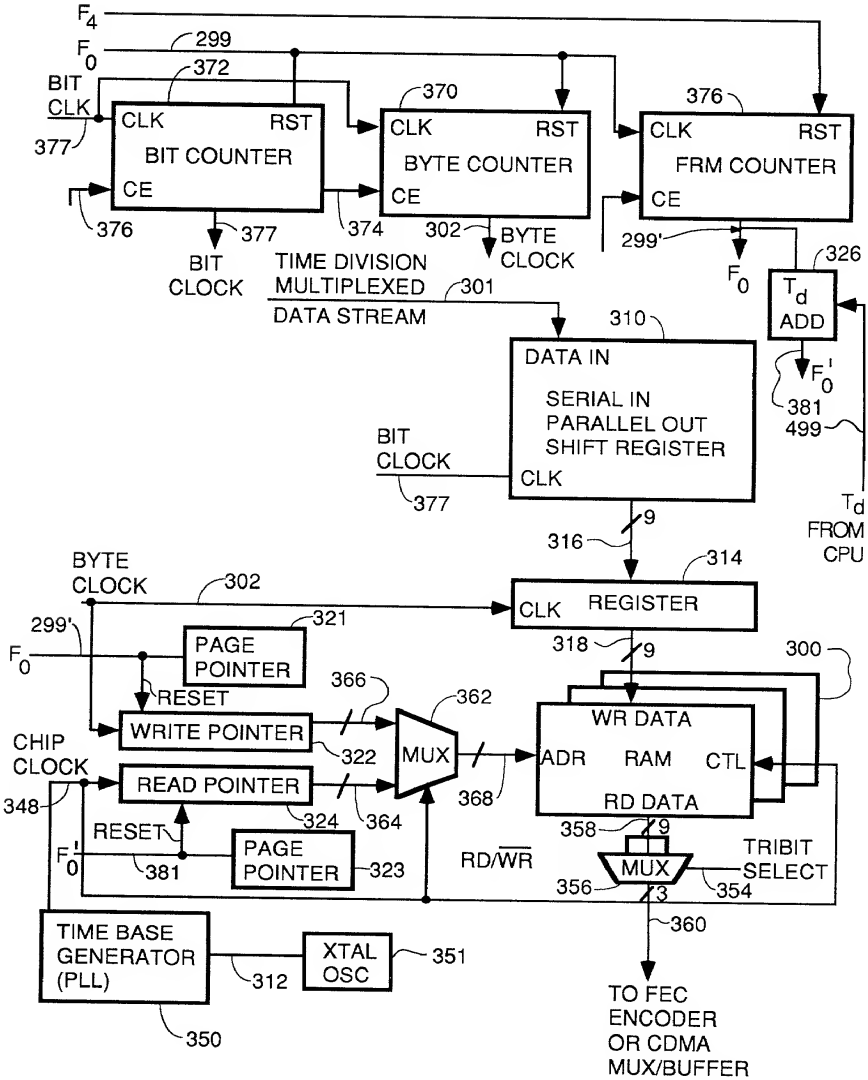

F4
F0
299
372
BIT CLK
377
CLK
RST
BIT COUNTER
CE
376
377
374
370
BYTE COUNTER
302
BYTE CLOCK
376
FRM COUNTER
299'
326
Td ADD
F'0
381
499
BIT CLOCK
TIME DIVISION MULTIPLEXED DATA STREAM
301
310
DATA IN
SERIAL IN PARALLEL OUT SHIFT REGISTER
CLK
377
9
316
314
REGISTER
Td FROM CPU
BYTE CLOCK
302
299'
321
PAGE POINTER
RESET
366
362
WRITE POINTER
322
MUX
CHIP CLOCK
READ POINTER
348
324
364
368
318
9
300
WR DATA
ADR
RAM
CTL
RD DATA
358
9
TRIBIT SELECT
MUX
356
3
354
360
RESET
F'0
381
PAGE POINTER
323
RD/WR
TIME BASE GENERATOR (PLL)
312
XTAL OSC
351
350
TO FEC ENCODER OR CDMA MUX/BUFFER

FIG. 9

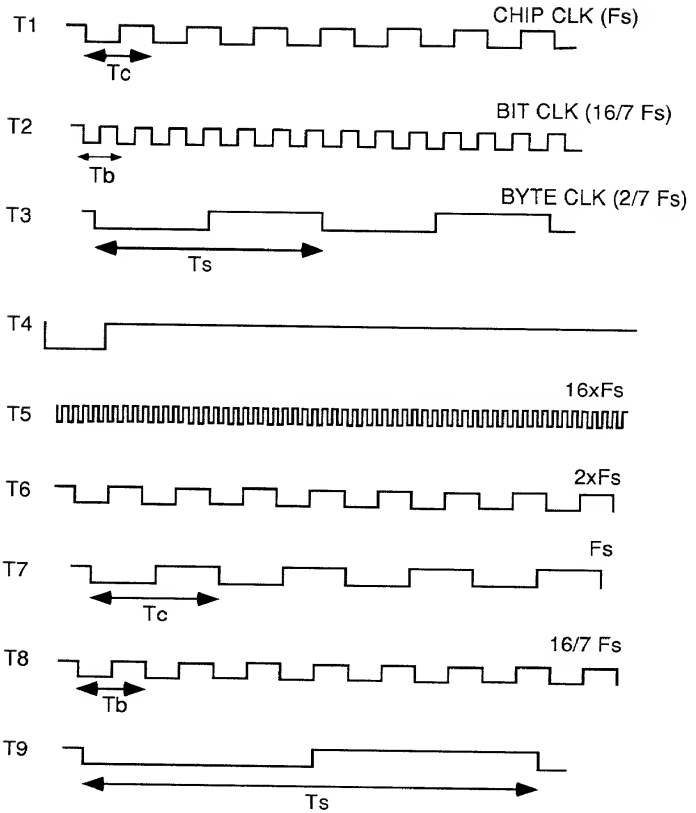

T1
CHIP CLK (Fs)
Tc
T2
BIT CLK (16/7 Fs)
Tb
T3
BYTE CLK (2/7 Fs)
Ts
T4
T5
16xFs
T6
2xFs
T7
Fs
Tc
T8
16/7 Fs
Tb
T9
Ts

FIG. 10

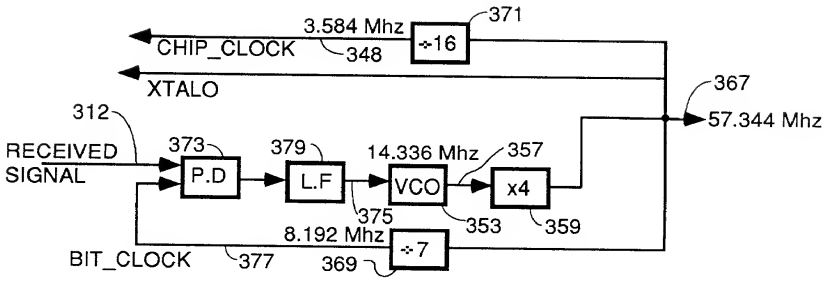


FIG. 11

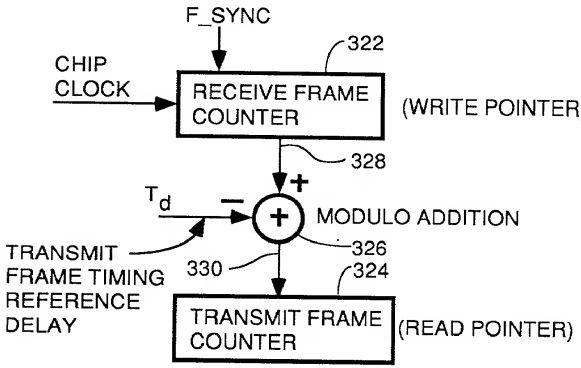


FIG. 12

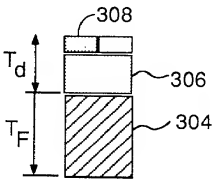


FIG. 13

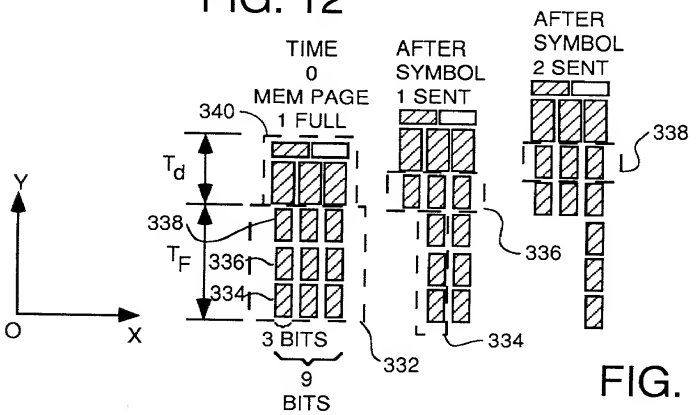


FIG. 14

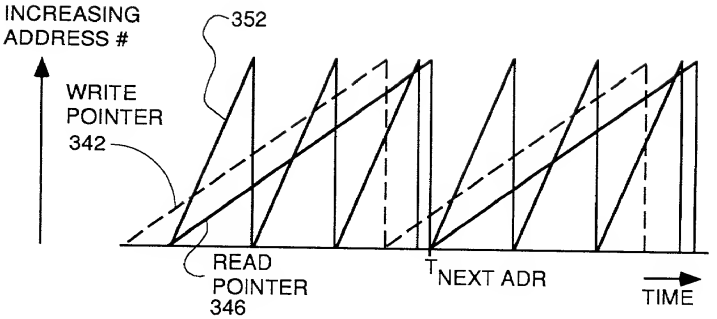

INCREASING
ADDRESS #
352
WRITE
POINTER
342
READ
POINTER
346
NEXT ADR
TIME

FIG. 15

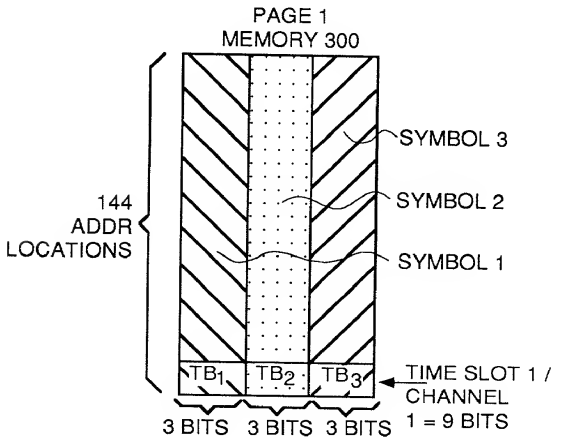
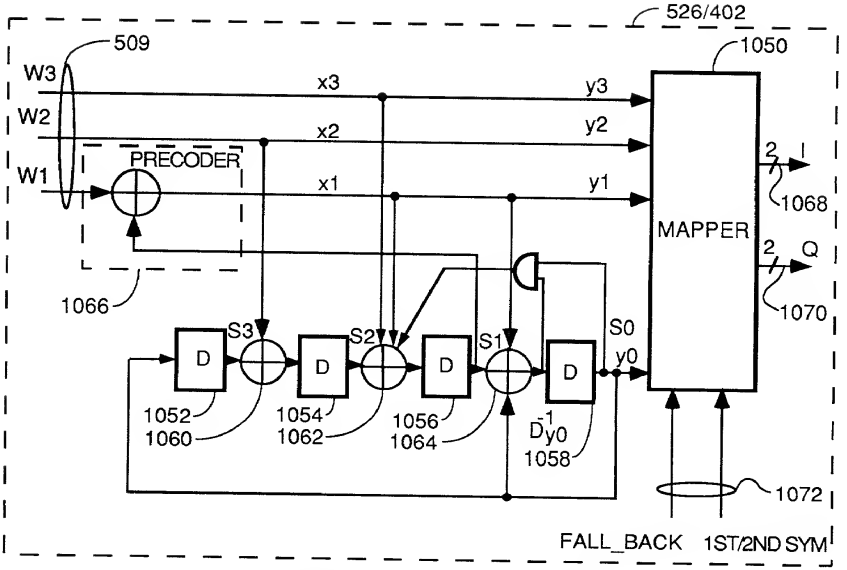

PAGE 1
MEMORY 300
144
ADDR
LOCATIONS
SYMBOL 3
SYMBOL 2
SYMBOL 1
TB1
TB2
TB3
TIME SLOT 1 /
CHANNEL
1 = 9 BITS
3 BITS
3 BITS
3 BITS

FIG. 16



PREFERRED TRELLIS ENCODER

FIG. 17

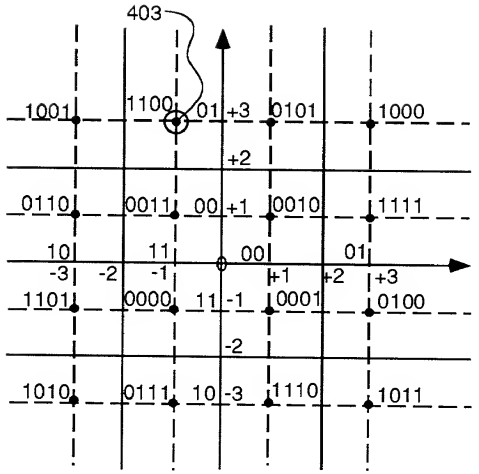


FIG. 18

	0000	111	111	
	0001	001	111	= 1 - j
	0010	001	001	= 1+ j
	0011	111	001	= -1+ j
	0100	011	111	= 3 - j
	0101	001	011	= 1+ 3* j
	0110	101	001	= -3 + j
	0111	111	101	= -1 - 3* j
	1000	011	011	=+3 + 3*j
	1001	101	011	= -3 + 3*j
	1010	101	101	= -3 - 3* j
	1011	011	101	= 3 - 3* j
403	1100	111	011	= -1+ 3* j
	1101	101	111	= -3 - j
	1110	001	101	= 1 - 3* j
	1111	011	001	= 3 + j

FIG. 19

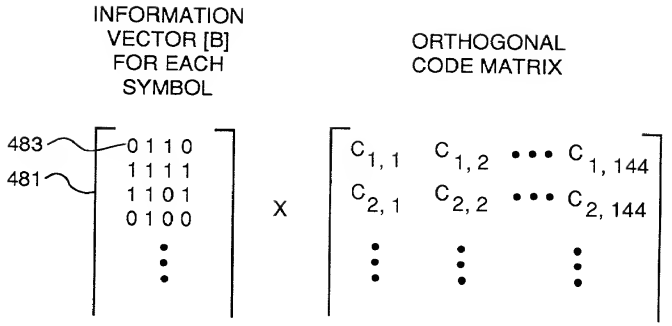


FIG. 20A

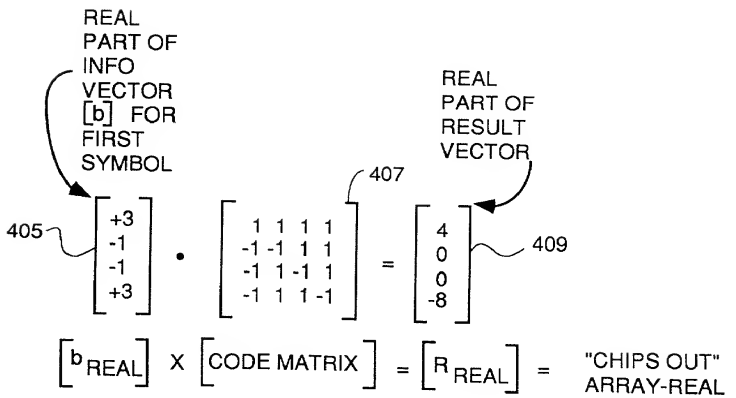


FIG. 20B

MAPPING FOR FALL-BACK MODE - LSB'S

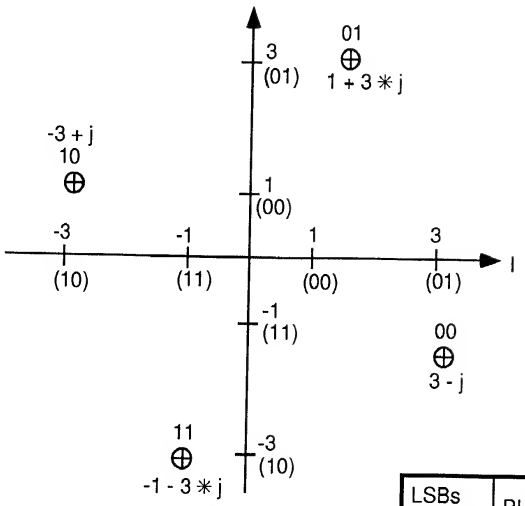


FIG. 21

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSB & MSB FALLBACK MODE MAPPINGS

FIG. 22

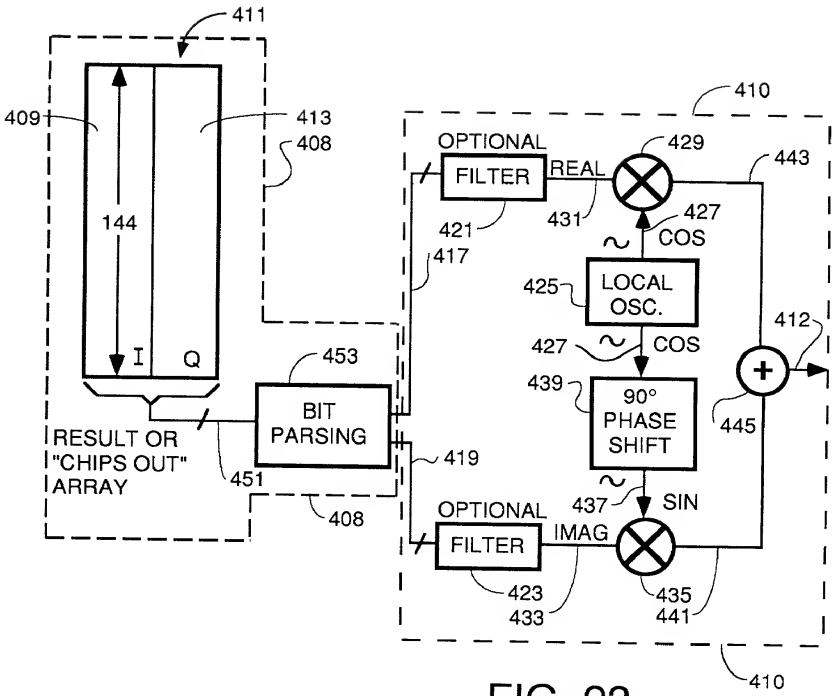

411
409
413
408
144
I
Q
453
BIT
PARSING
RESULT OR
"CHIPS OUT"
ARRAY
451
408
410
OPTIONAL
FILTER
REAL
429
443
421
431
427
COS
417
425
LOCAL
OSC.
412
427
COS
439
90°
PHASE
SHIFT
445
419
437
SIN
OPTIONAL
FILTER
IMAG
423
433
435
441
410

FIG. 23

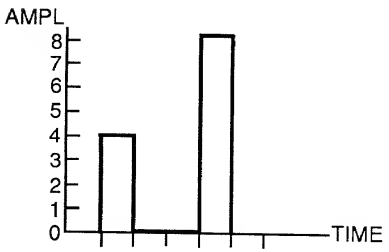

AMPL
8
7
6
5
4
3
2
1
0
TIME

FIG. 24

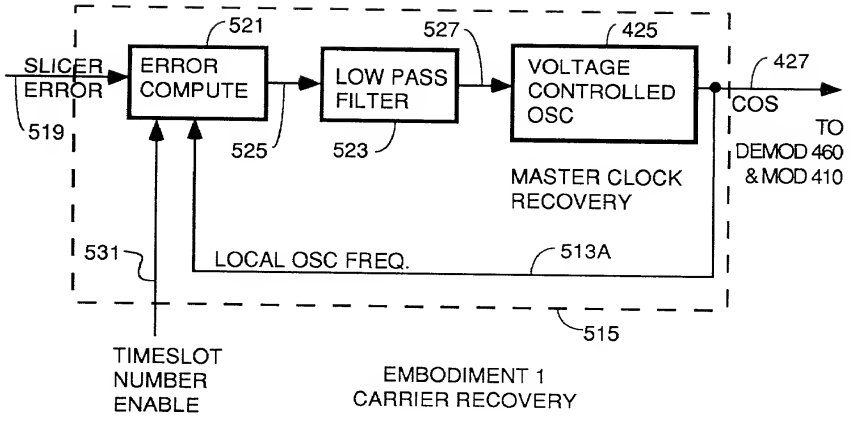

521
527
425
SLICER ERROR
ERROR COMPUTE
LOW PASS FILTER
VOLTAGE CONTROLLED OSC
427
COS
TO DEMOD 460 & MOD 410
519
525
523
MASTER CLOCK RECOVERY
531
LOCAL OSC FREQ.
513A
515
TIMESLOT NUMBER ENABLE
EMBODIMENT 1 CARRIER RECOVERY

FIG. 25

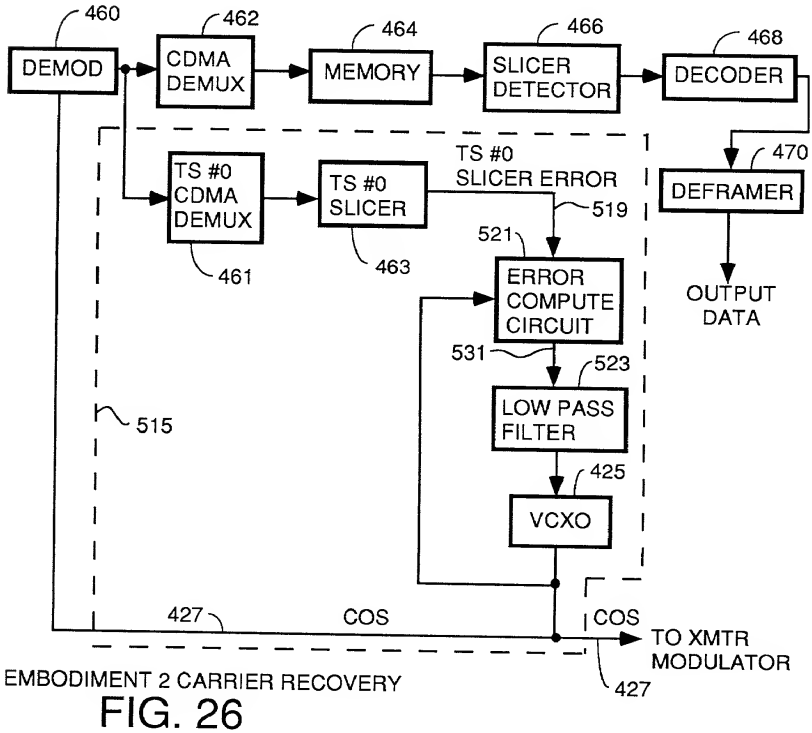

460
462
464
466
468
DEMOD
CDMA DEMUX
MEMORY
SLICER DETECTOR
DECODER
TS #0 CDMA DEMUX
TS #0 SLICER
TS #0 SLICER ERROR
470
DEFRAMER
519
521
461
463
ERROR COMPUTE CIRCUIT
OUTPUT DATA
531
523
LOW PASS FILTER
515
425
VCXO
427
COS
COS
TO XMTR MODULATOR
EMBODIMENT 2 CARRIER RECOVERY
427

FIG. 26

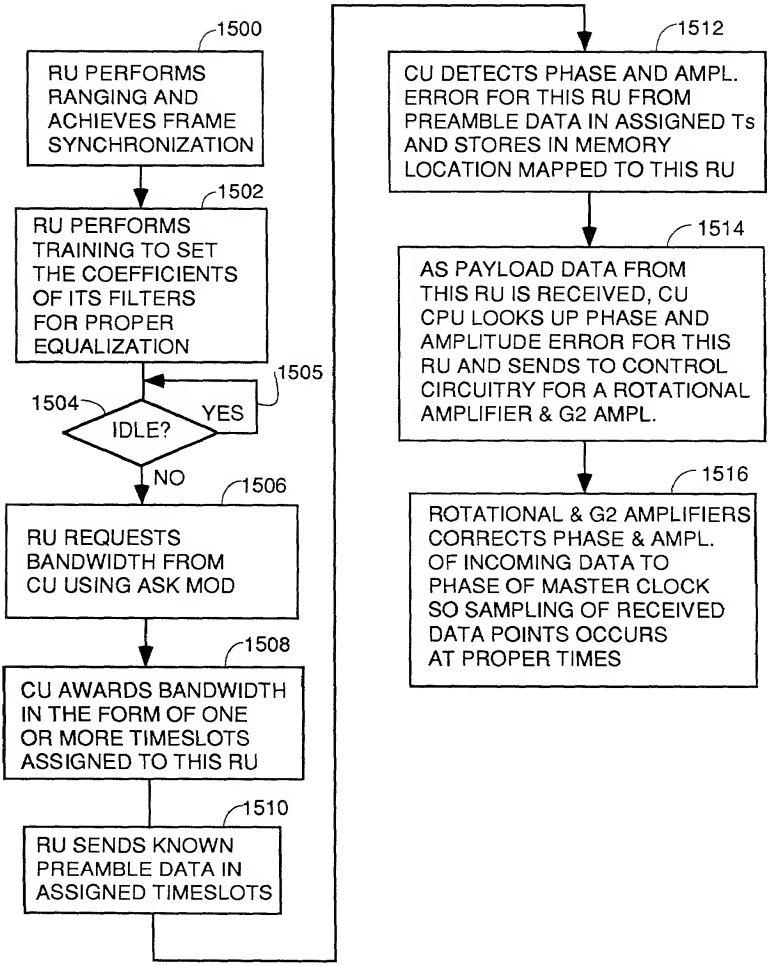
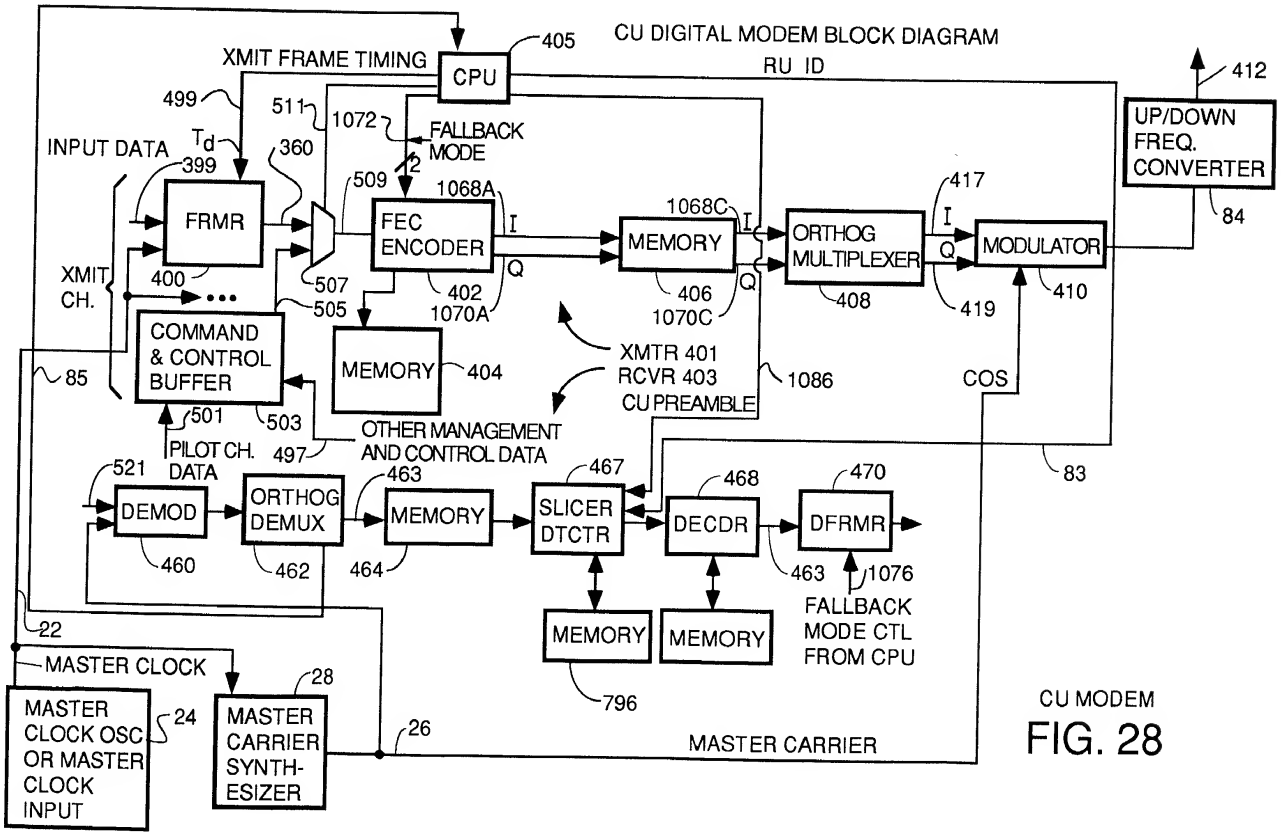

1500
RU PERFORMS RANGING AND ACHIEVES FRAME SYNCHRONIZATION
1502
RU PERFORMS TRAINING TO SET THE COEFFICIENTS OF ITS FILTERS FOR PROPER EQUALIZATION
1505
1504
IDLE?
YES
NO
1506
RU REQUESTS BANDWIDTH FROM CU USING ASK MOD
1508
CU AWARDS BANDWIDTH IN THE FORM OF ONE OR MORE TIMESLOTS ASSIGNED TO THIS RU
1510
RU SENDS KNOWN PREAMBLE DATA IN ASSIGNED TIMESLOTS
1512
CU DETECTS PHASE AND AMPL. ERROR FOR THIS RU FROM PREAMBLE DATA IN ASSIGNED Ts AND STORES IN MEMORY LOCATION MAPPED TO THIS RU
1514
AS PAYLOAD DATA FROM THIS RU IS RECEIVED, CU CPU LOOKS UP PHASE AND AMPLITUDE ERROR FOR THIS RU AND SENDS TO CONTROL CIRCUITRY FOR A ROTATIONAL AMPLIFIER & G2 AMPL.
1516
ROTATIONAL & G2 AMPLIFIERS CORRECTS PHASE & AMPL. OF INCOMING DATA TO PHASE OF MASTER CLOCK SO SAMPLING OF RECEIVED DATA POINTS OCCURS AT PROPER TIMES

FIG. 27



CU MODEM

FIG. 28

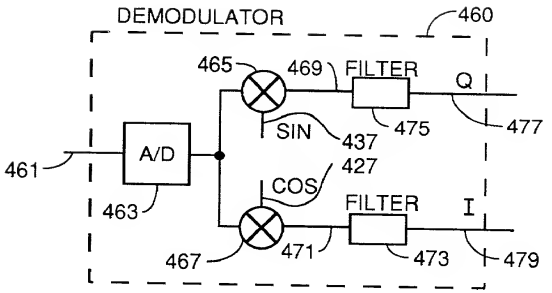

DEMODULATOR
460
465
469
FILTER
Q
SIN
437
475
477
461
A/D
427
COS
463
FILTER
I
467
471
473
479

FIG. 29

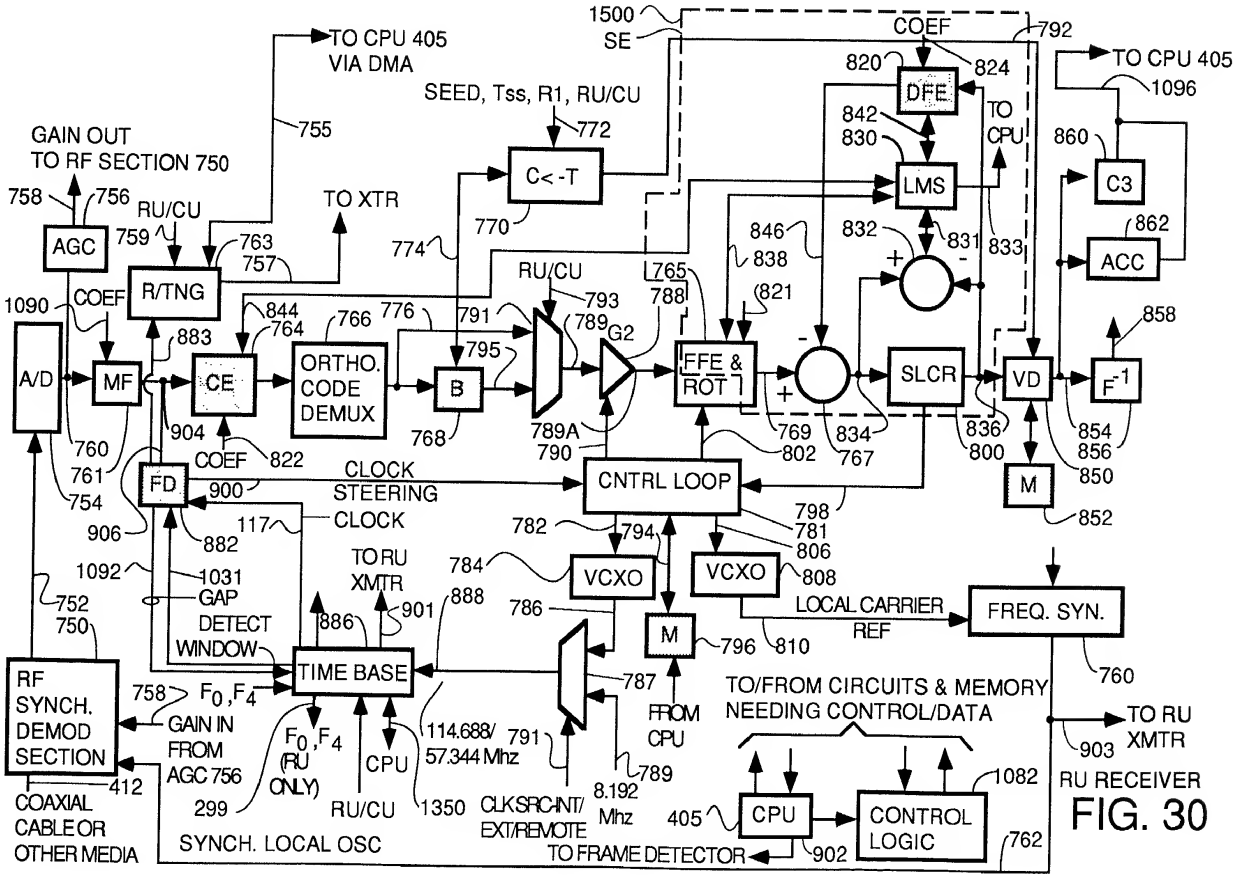
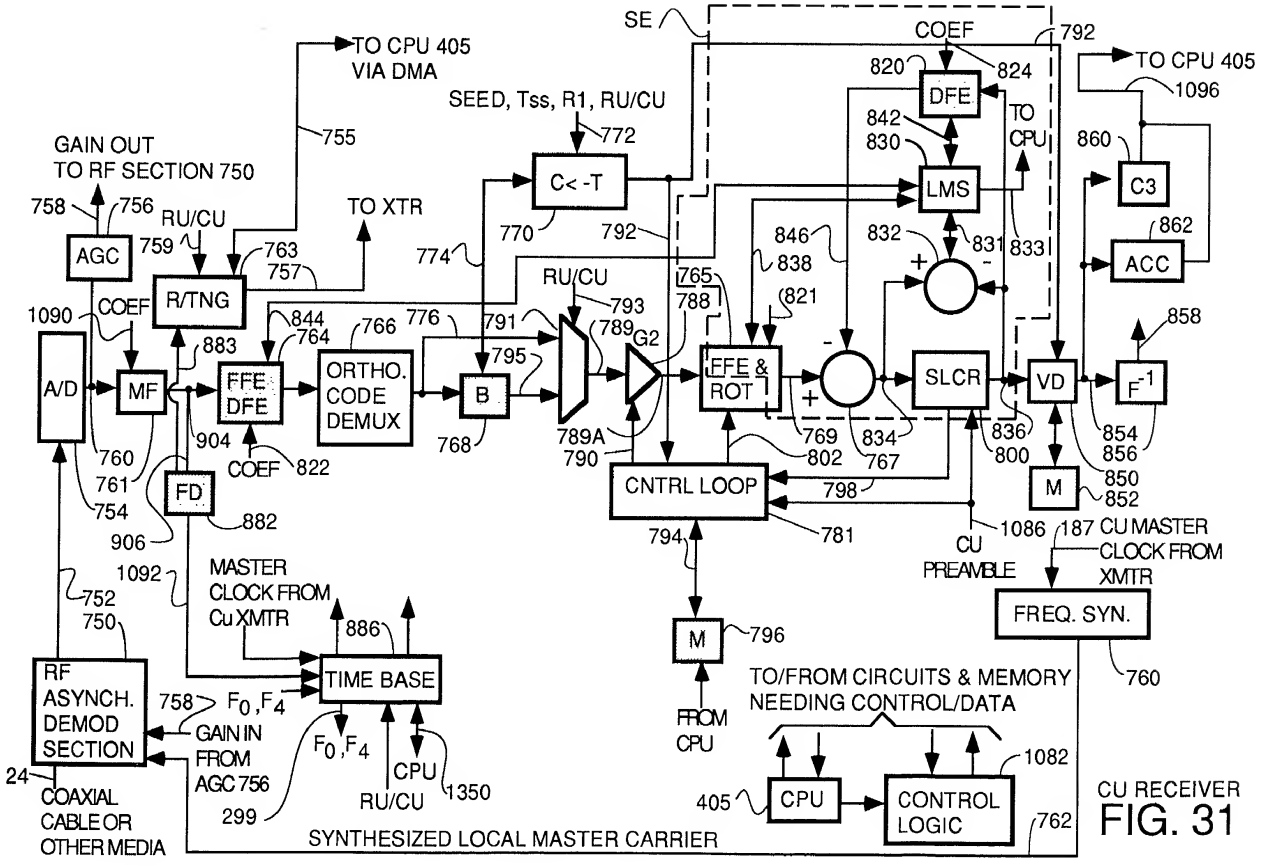
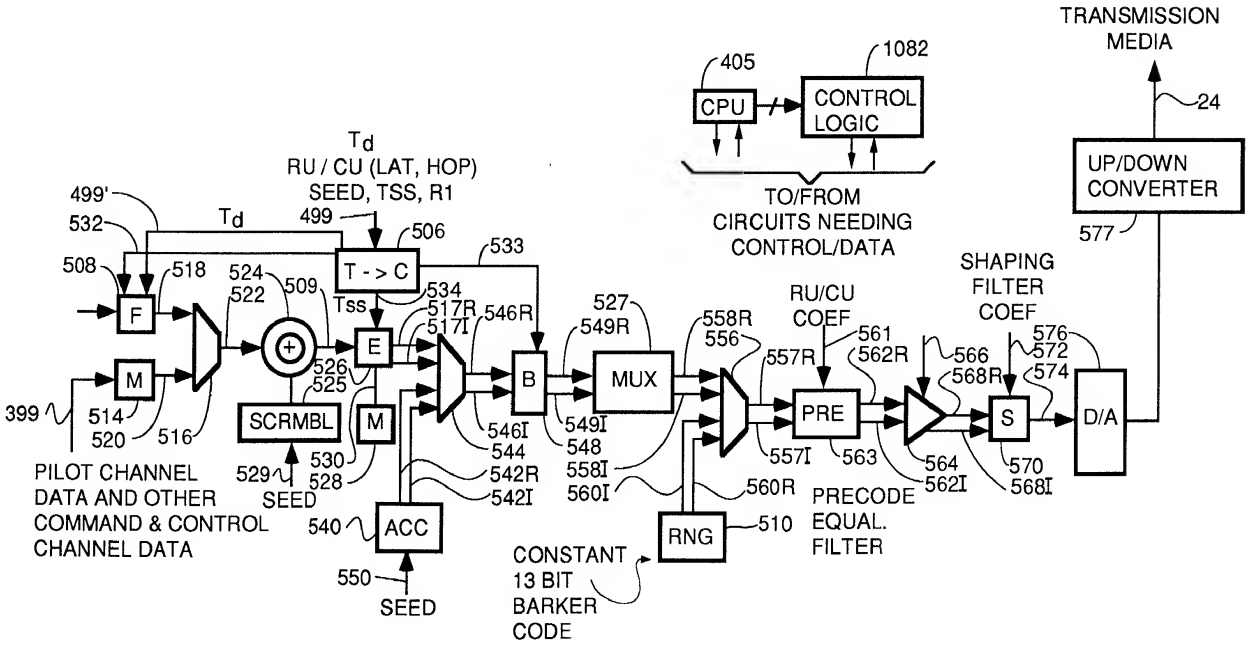

1500
SE
COEF
792
TO CPU 405
VIA DMA
820
824
DFE
TO CPU 405
1096
SEED, Tss, R1, RU/CU
772
842
830
TO CPU
860
GAIN OUT
TO RF SECTION 750
755
C<-T
LMS
C3
758
756
RU/CU
TO XTR
770
846
832
862
759
763
757
774
838
831
833
ACC
AGC
R/TNG
RU/CU
765
788
821
1090
COEF
844
764
766
776
791
793
789
G2
795
858
883
A/D
MF
CE
ORTHO. CODE DEMUX
B
FFE & ROT
SLCR
VD
F-1
904
768
789A
790
769
834
836
854
760
COEF
822
802
767
800
856
761
CLOCK STEERING
CNTRL LOOP
M
850
754
FD
900
798
906
117
CLOCK
782
794
781
852
882
806
1092
1031
TO RU XMTR
784
VCXO
VCXO
808
752
GAP
888
786
LOCAL CARRIER REF
FREQ. SYN.
750
DETECT WINDOW
886
901
M
796
810
760
RF SYNCH. DEMOD SECTION
758
F0,F4
TIME BASE
787
TO/FROM CIRCUITS & MEMORY NEEDING CONTROL/DATA
GAIN IN FROM AGC 756
F0,F4 (RU ONLY)
CPU
114.688/ 57.344 Mhz
791
FROM CPU
TO RU XMTR
903
412
299
RU/CU
1350
CLKSRC=INT/ EXT/REMOTE
8.192 Mhz
789
RU RECEIVER
405
CPU
1082
CONTROL LOGIC
COAXIAL CABLE OR OTHER MEDIA
SYNCH. LOCAL OSC
TO FRAME DETECTOR
902
762

FIG. 30



CU RECEIVER
FIG. 31



CU TRANSMITTER

FIG. 32

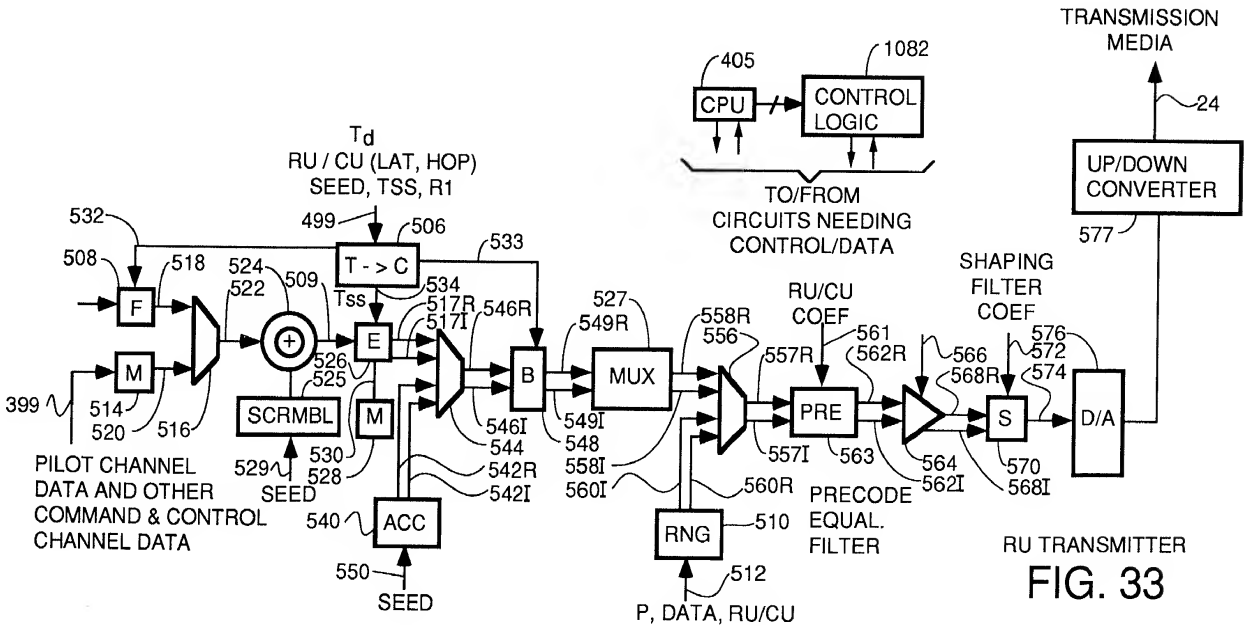


FIG. 33

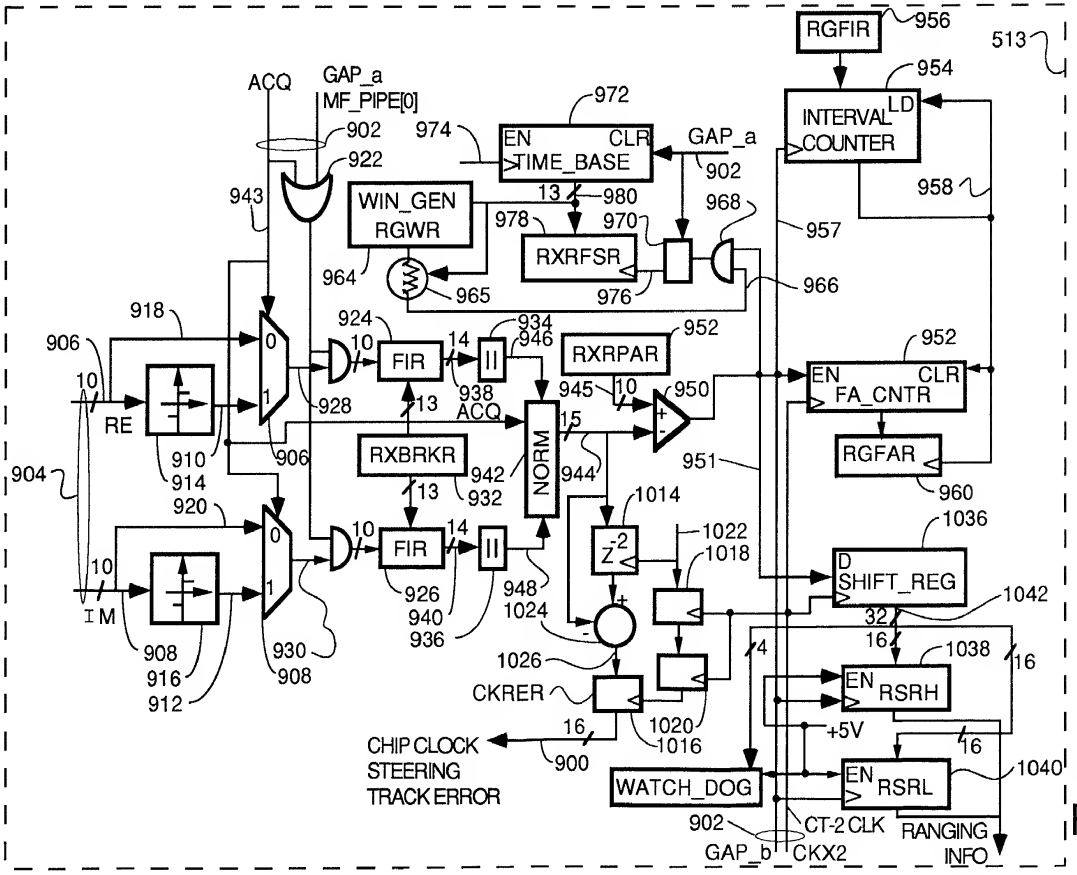

RGFIR
956
513
954
INTERVAL COUNTER
LD
958
957
ACQ
GAP_a
MF_PIPE[0]
902
922
943
972
974
EN CLR
TIME_BASE
GAP_a
902
WIN_GEN
RGWR
13
980
978
970
968
RXRFSR
964
965
976
966
918
906
924
10
FIR
14
934
946
RXRPAR
952
952
EN CLR
FA_CNTR
10
RE
928
13
938
ACQ
945
10
950
RXBRKR
942
932
NORM
15
944
951
RGFAR
960
904
910
914
906
920
1014
1036
10
FIR
14
1022
1018
D
SHIFT_REG
1042
32
16
I M
926
940
936
948
1024
908
916
912
930
908
1026
4
1038
16
EN RSRH
CKRER
1020
1016
+5V
16
16
CHIP CLOCK
STEERING
TRACK ERROR
900
WATCH_DOG
EN RSRL
1040
902
GAP_b
CT-2 CLK
CKX2
RANGING
INFO
FRAME
DETECTOR/
RANGING
DETECTOR

FIG. 34

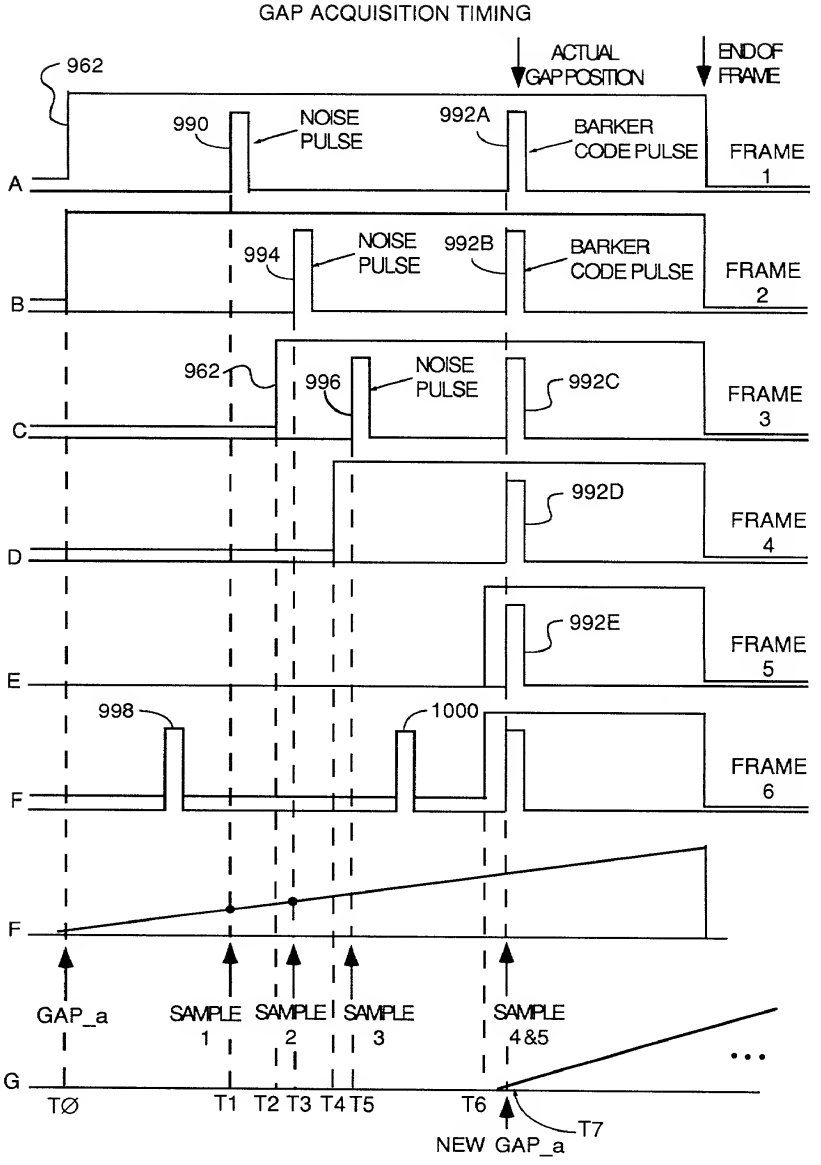

GAP ACQUISITION TIMING
ACTUAL GAP POSITION
END OF FRAME
962
990
NOISE PULSE
992A
BARKER CODE PULSE
FRAME 1
A
994
NOISE PULSE
992B
BARKER CODE PULSE
FRAME 2
B
962
996
NOISE PULSE
992C
FRAME 3
C
992D
FRAME 4
D
992E
FRAME 5
E
998
1000
FRAME 6
F
F
GAP_a
SAMPLE 1
SAMPLE 2
SAMPLE 3
SAMPLE 4&5
G
TØ
T1 T2 T3 T4 T5
T6
T7
NEW GAP_a

FIG. 35

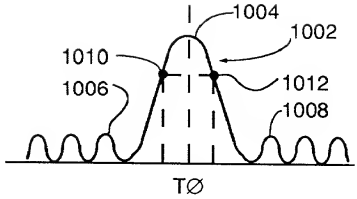


FIG. 36

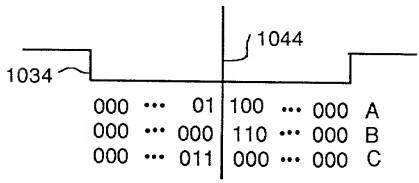


FIG. 37
FINE TUNING TO
CENTER BARKER CODE

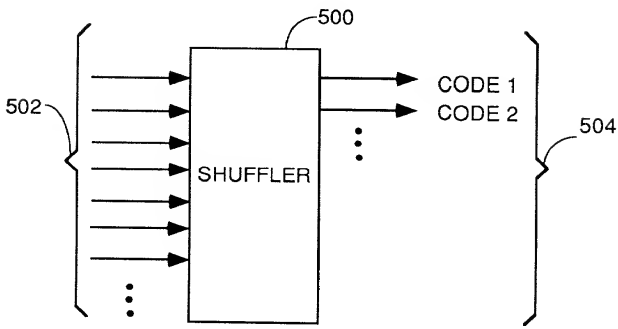


FIG. 38

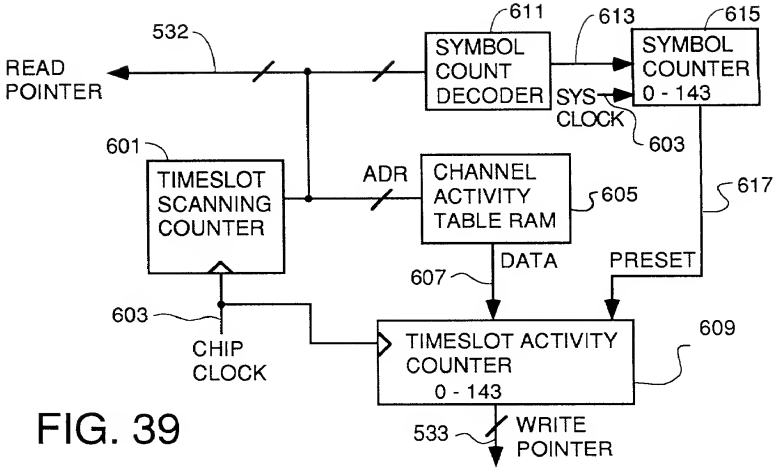


FIG. 39

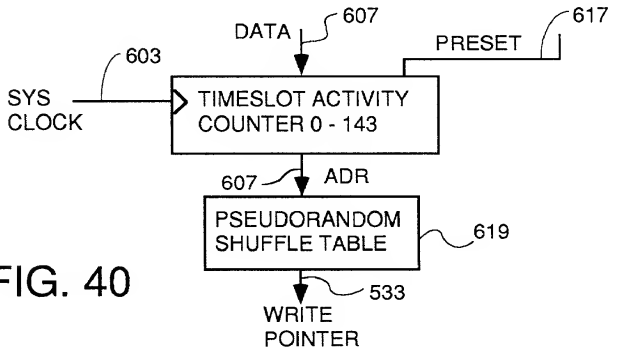


FIG. 40

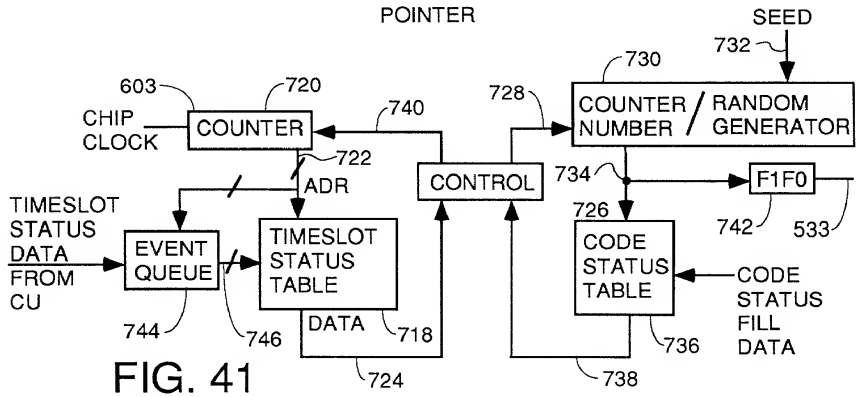


FIG. 41

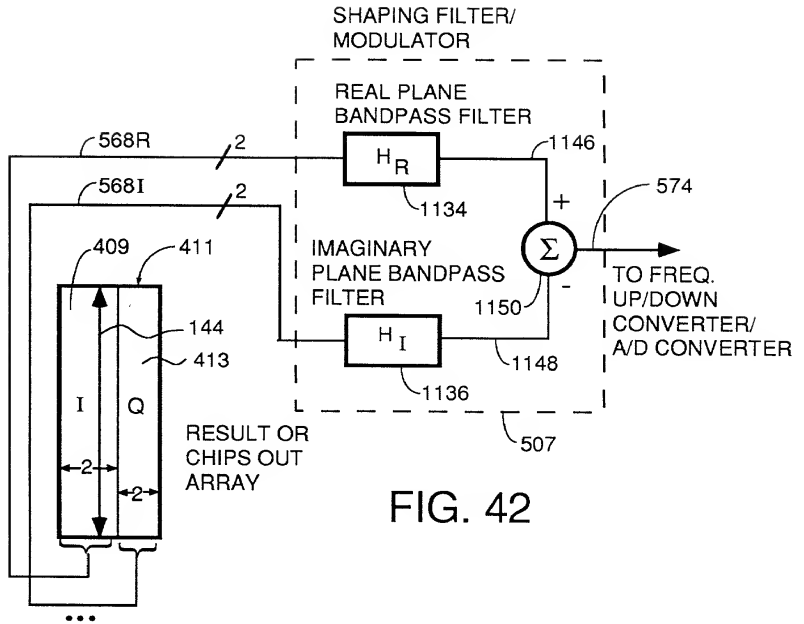


FIG. 42

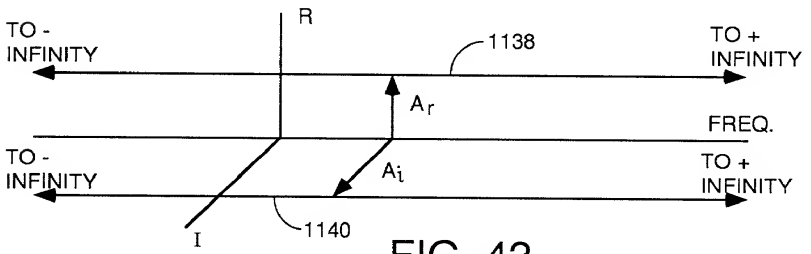


FIG. 43

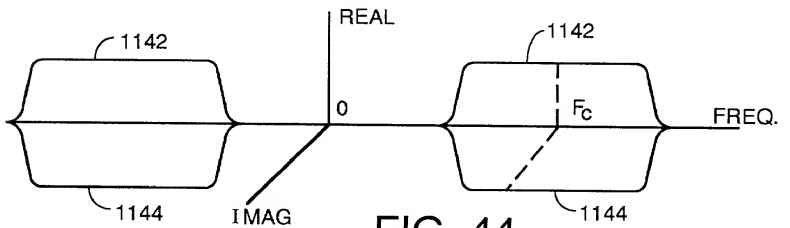
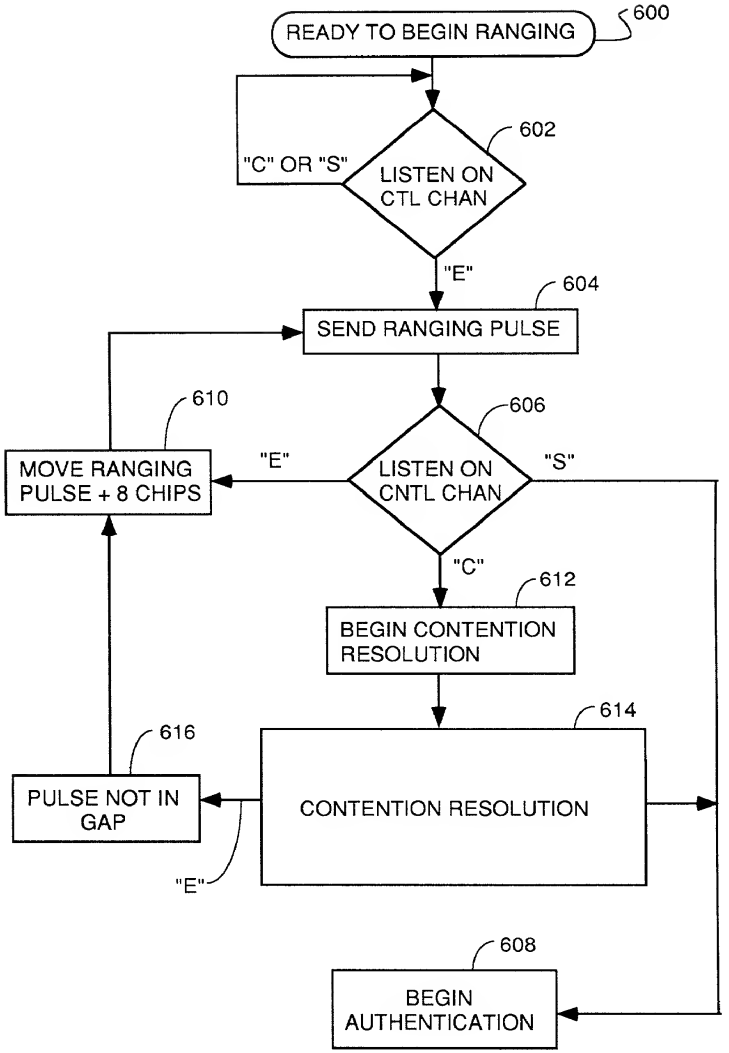
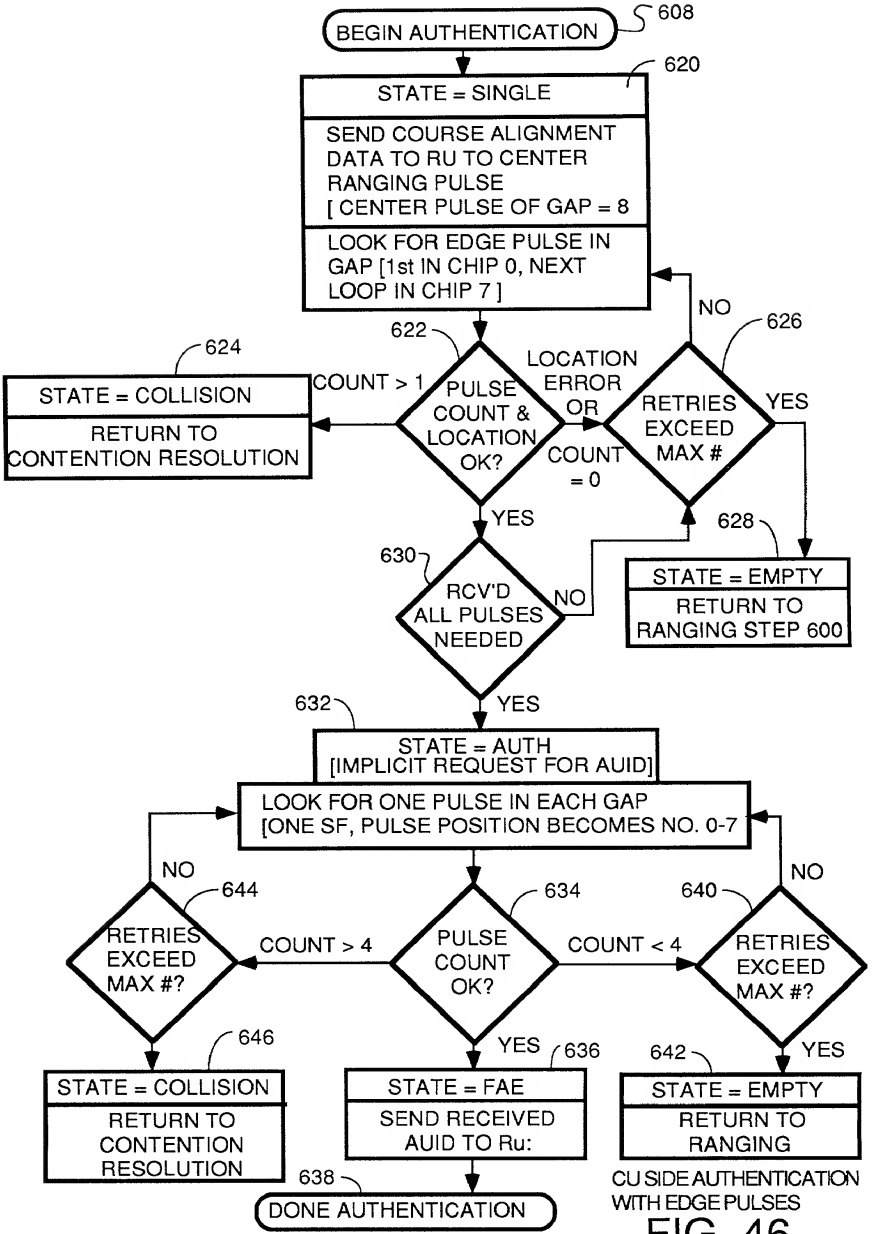


FIG. 44



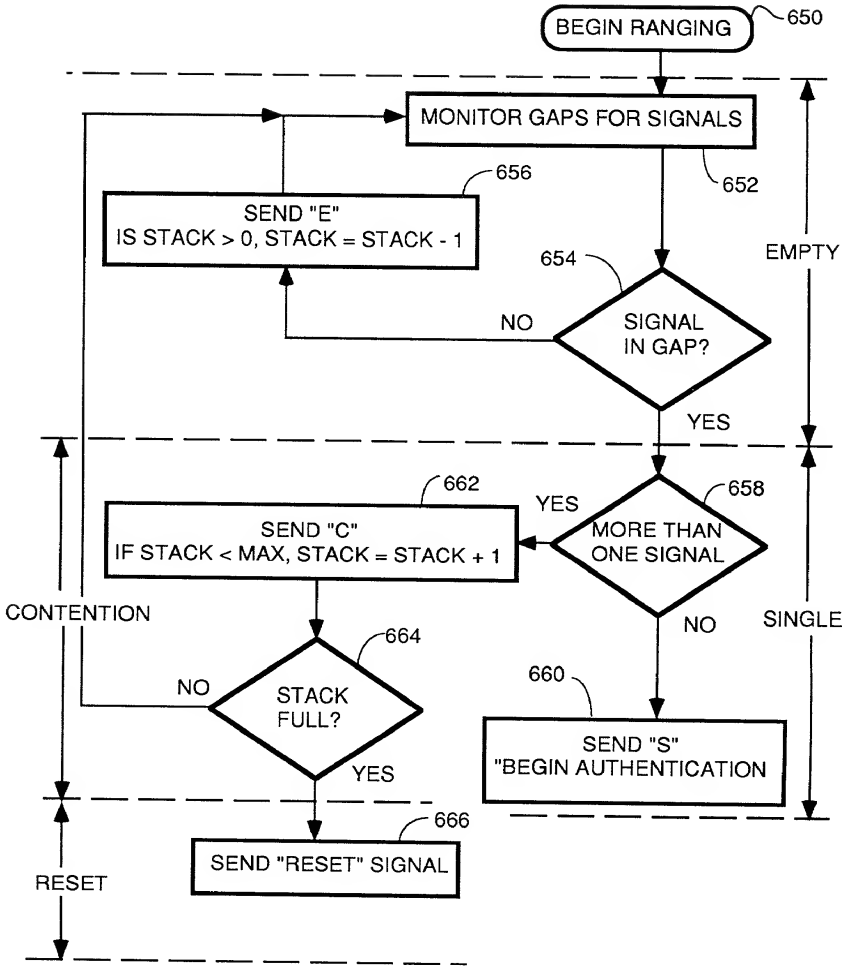
RU RANGING

FIG. 45



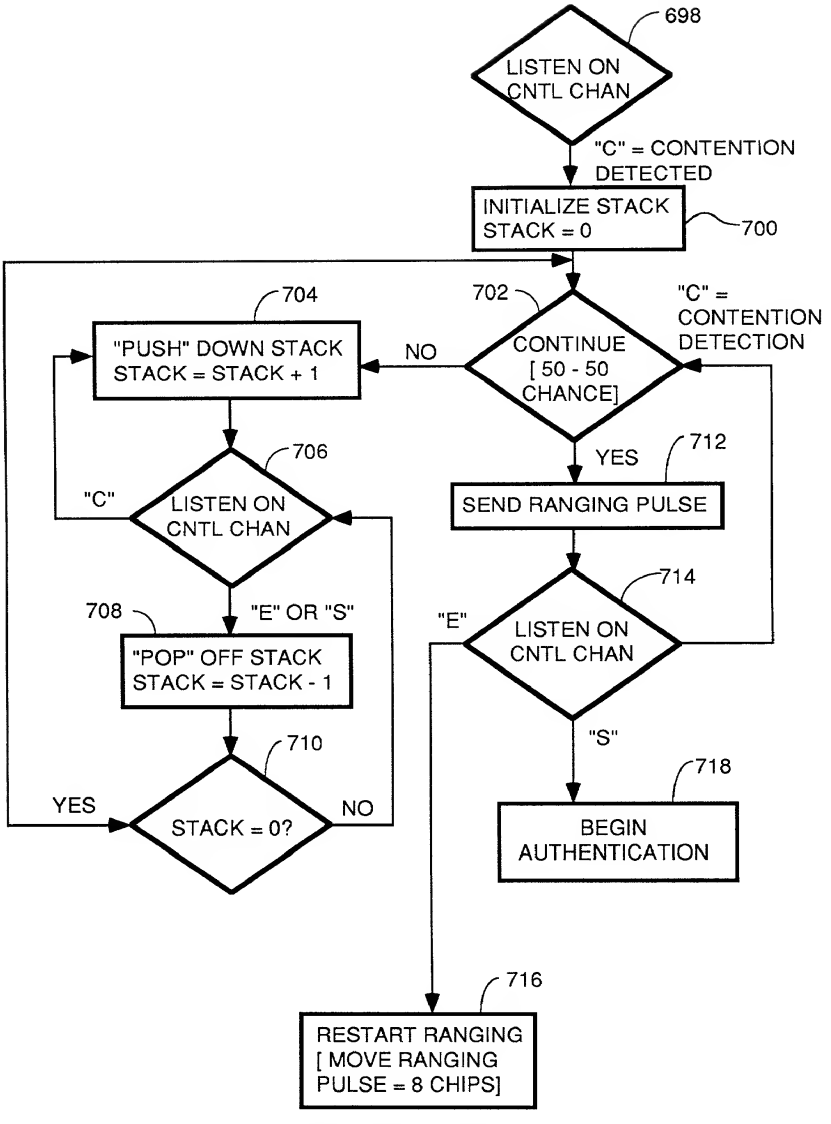
CU SIDE AUTHENTICATION WITH EDGE PULSES

FIG. 46



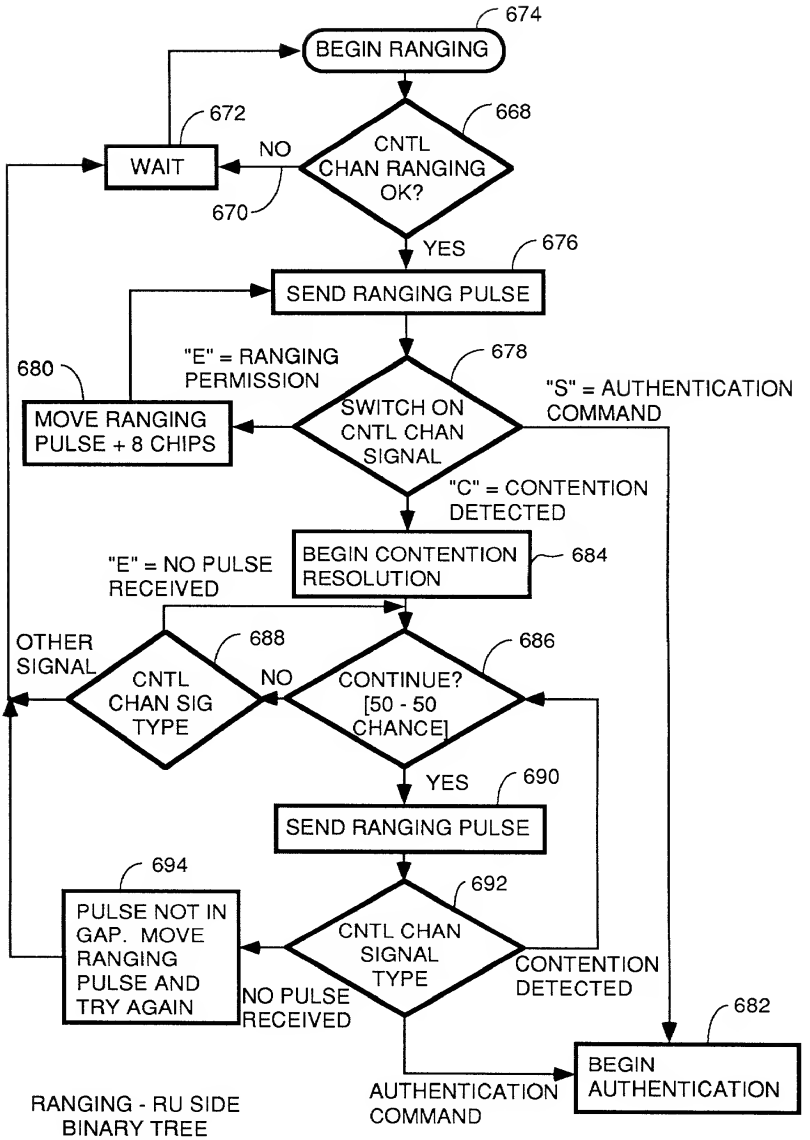
CU RANGING AND CONTENTION RESOLUTION

FIG. 47



CONTENTION RESOLUTION - RU USING BINARY STACK

FIG. 48



RANGING - RU SIDE BINARY TREE ALGORITHM

FIG. 49

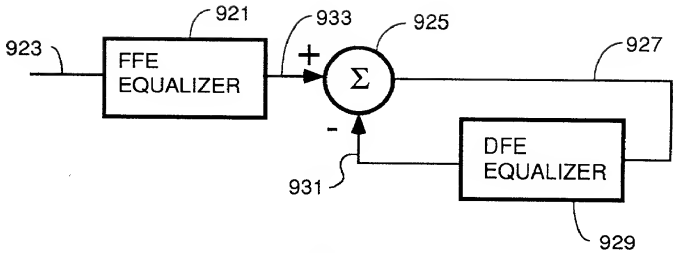


FIG. 50

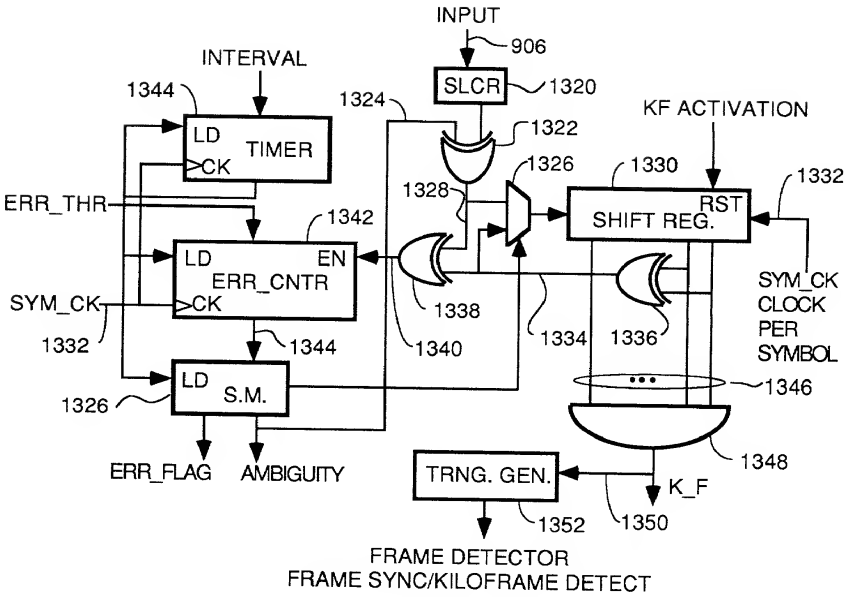
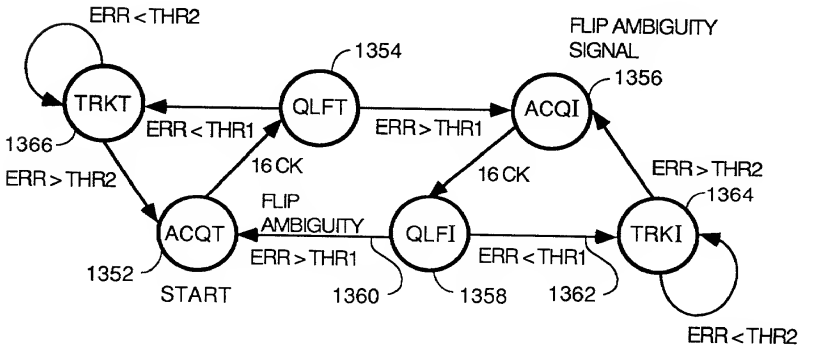


FIG. 51



STATE MACHINE

FIG. 52

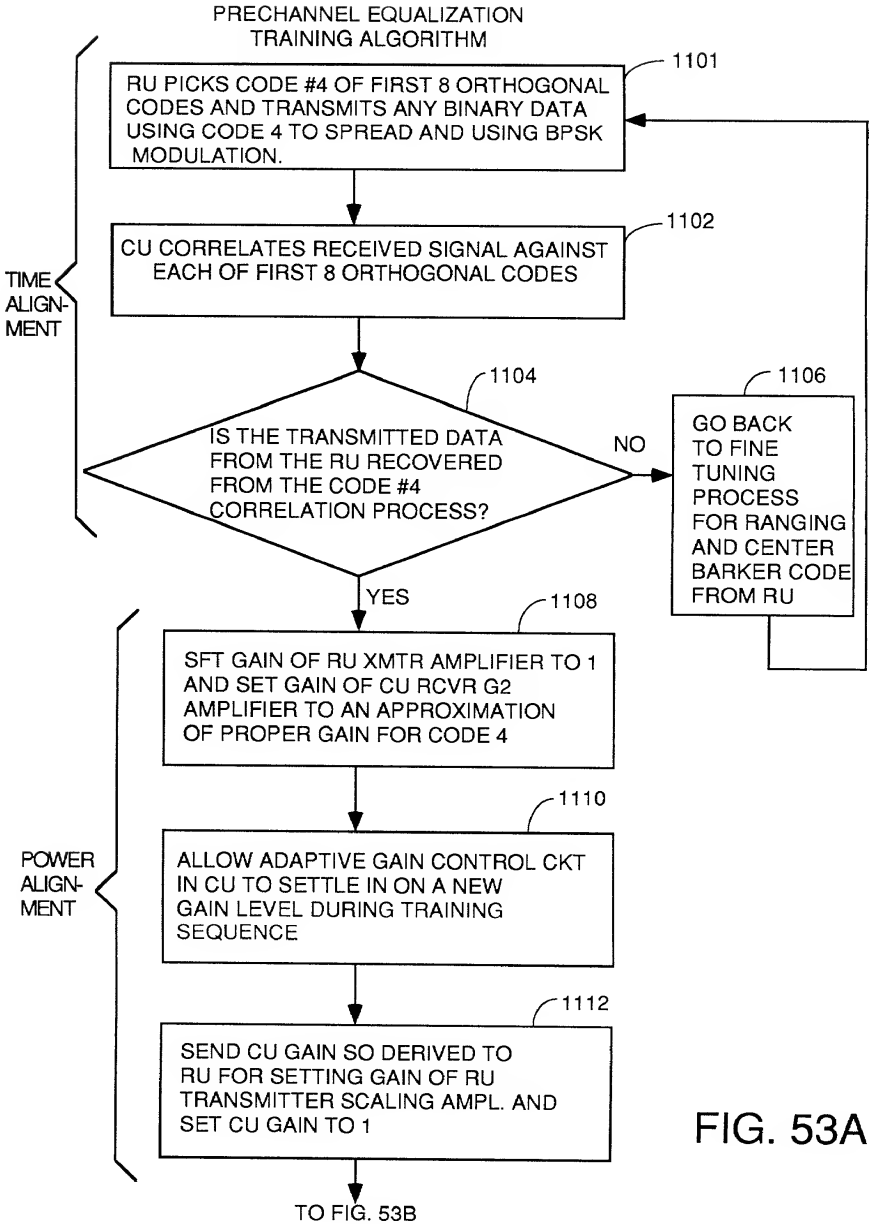

PRECHANNEL EQUALIZATION TRAINING ALGORITHM
1101
RU PICKS CODE #4 OF FIRST 8 ORTHOGONAL CODES AND TRANSMITS ANY BINARY DATA USING CODE 4 TO SPREAD AND USING BPSK MODULATION.
1102
CU CORRELATES RECEIVED SIGNAL AGAINST EACH OF FIRST 8 ORTHOGONAL CODES
TIME ALIGN-MENT
1104
IS THE TRANSMITTED DATA FROM THE RU RECOVERED FROM THE CODE #4 CORRELATION PROCESS?
NO
1106
GO BACK TO FINE TUNING PROCESS FOR RANGING AND CENTER BARKER CODE FROM RU
YES
1108
SFT GAIN OF RU XMTR AMPLIFIER TO 1 AND SET GAIN OF CU RCVR G2 AMPLIFIER TO AN APPROXIMATION OF PROPER GAIN FOR CODE 4
1110
ALLOW ADAPTIVE GAIN CONTROL CKT IN CU TO SETTLE IN ON A NEW GAIN LEVEL DURING TRAINING SEQUENCE
POWER ALIGN-MENT
1112
SEND CU GAIN SO DERIVED TO RU FOR SETTING GAIN OF RU TRANSMITTER SCALING AMPL. AND SET CU GAIN TO 1
TO FIG. 53B

FIG. 53A

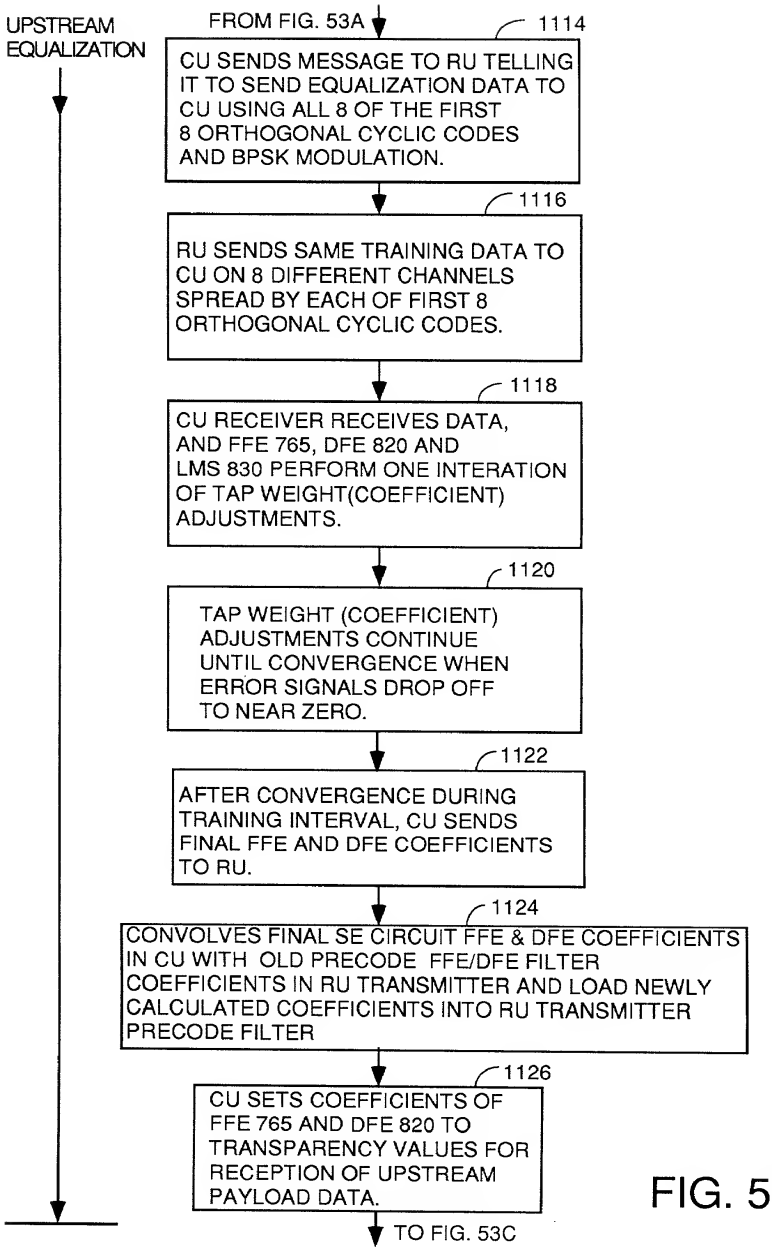

UPSTREAM EQUALIZATION
FROM FIG. 53A
1114
CU SENDS MESSAGE TO RU TELLING IT TO SEND EQUALIZATION DATA TO CU USING ALL 8 OF THE FIRST 8 ORTHOGONAL CYCLIC CODES AND BPSK MODULATION.
1116
RU SENDS SAME TRAINING DATA TO CU ON 8 DIFFERENT CHANNELS SPREAD BY EACH OF FIRST 8 ORTHOGONAL CYCLIC CODES.
1118
CU RECEIVER RECEIVES DATA, AND FFE 765, DFE 820 AND LMS 830 PERFORM ONE INTERATION OF TAP WEIGHT(COEFFICIENT) ADJUSTMENTS.
1120
TAP WEIGHT (COEFFICIENT) ADJUSTMENTS CONTINUE UNTIL CONVERGENCE WHEN ERROR SIGNALS DROP OFF TO NEAR ZERO.
1122
AFTER CONVERGENCE DURING TRAINING INTERVAL, CU SENDS FINAL FFE AND DFE COEFFICIENTS TO RU.
1124
CONVOLVES FINAL SE CIRCUIT FFE & DFE COEFFICIENTS IN CU WITH OLD PRECODE FFE/DFE FILTER COEFFICIENTS IN RU TRANSMITTER AND LOAD NEWLY CALCULATED COEFFICIENTS INTO RU TRANSMITTER PRECODE FILTER
1126
CU SETS COEFFICIENTS OF FFE 765 AND DFE 820 TO TRANSPARENCY VALUES FOR RECEPTION OF UPSTREAM PAYLOAD DATA.
TO FIG. 53C

FIG. 53B

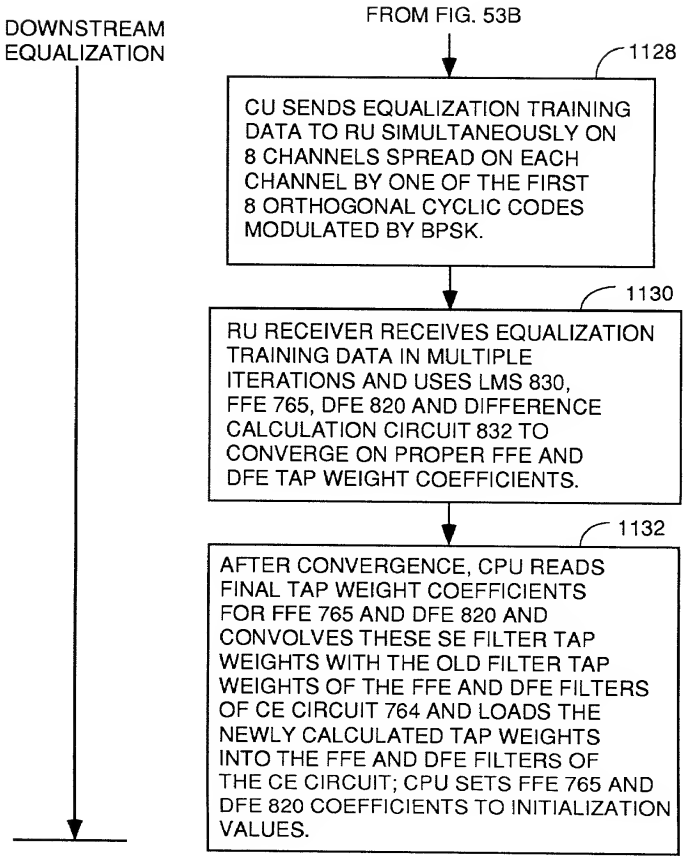

DOWNSTREAM EQUALIZATION
FROM FIG. 53B
1128
CU SENDS EQUALIZATION TRAINING DATA TO RU SIMULTANEOUSLY ON 8 CHANNELS SPREAD ON EACH CHANNEL BY ONE OF THE FIRST 8 ORTHOGONAL CYCLIC CODES MODULATED BY BPSK.
1130
RU RECEIVER RECEIVES EQUALIZATION TRAINING DATA IN MULTIPLE ITERATIONS AND USES LMS 830, FFE 765, DFE 820 AND DIFFERENCE CALCULATION CIRCUIT 832 TO CONVERGE ON PROPER FFE AND DFE TAP WEIGHT COEFFICIENTS.
1132
AFTER CONVERGENCE, CPU READS FINAL TAP WEIGHT COEFFICIENTS FOR FFE 765 AND DFE 820 AND CONVOLVES THESE SE FILTER TAP WEIGHTS WITH THE OLD FILTER TAP WEIGHTS OF THE FFE AND DFE FILTERS OF CE CIRCUIT 764 AND LOADS THE NEWLY CALCULATED TAP WEIGHTS INTO THE FFE AND DFE FILTERS OF THE CE CIRCUIT; CPU SETS FFE 765 AND DFE 820 COEFFICIENTS TO INITIALIZATION VALUES.

FIG. 53C

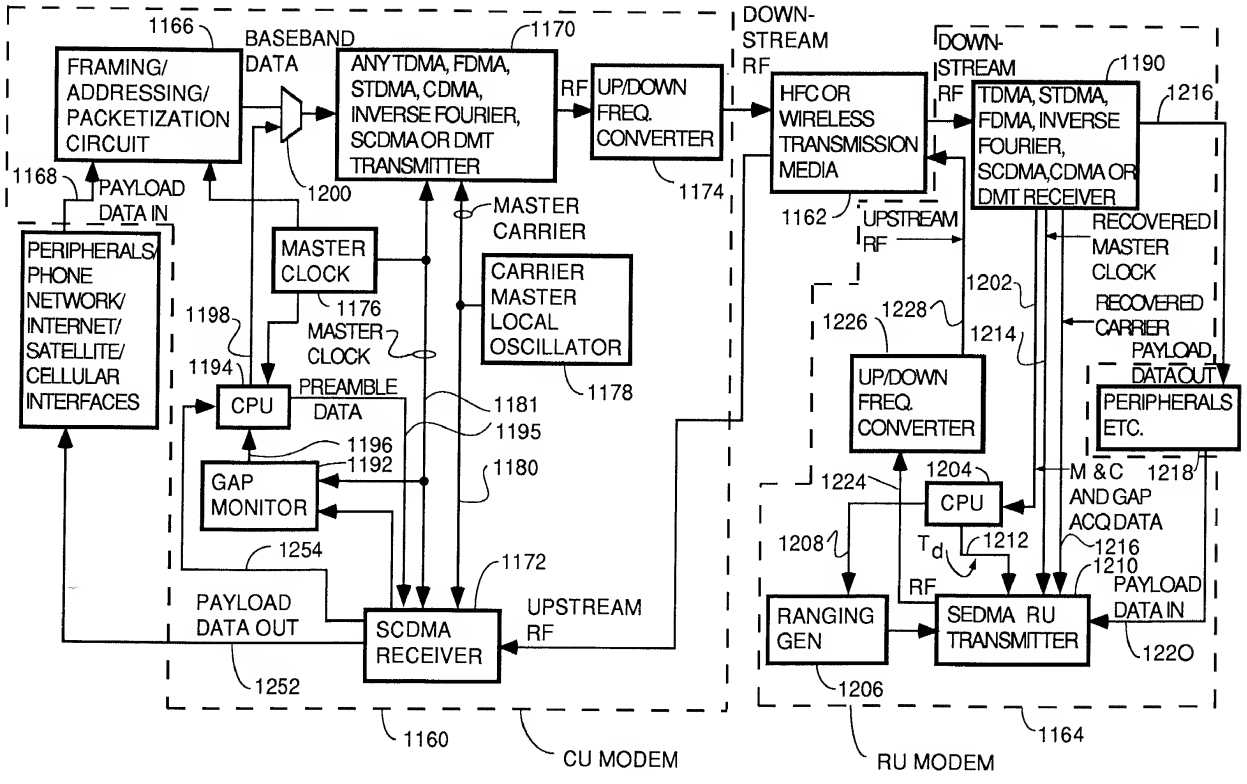
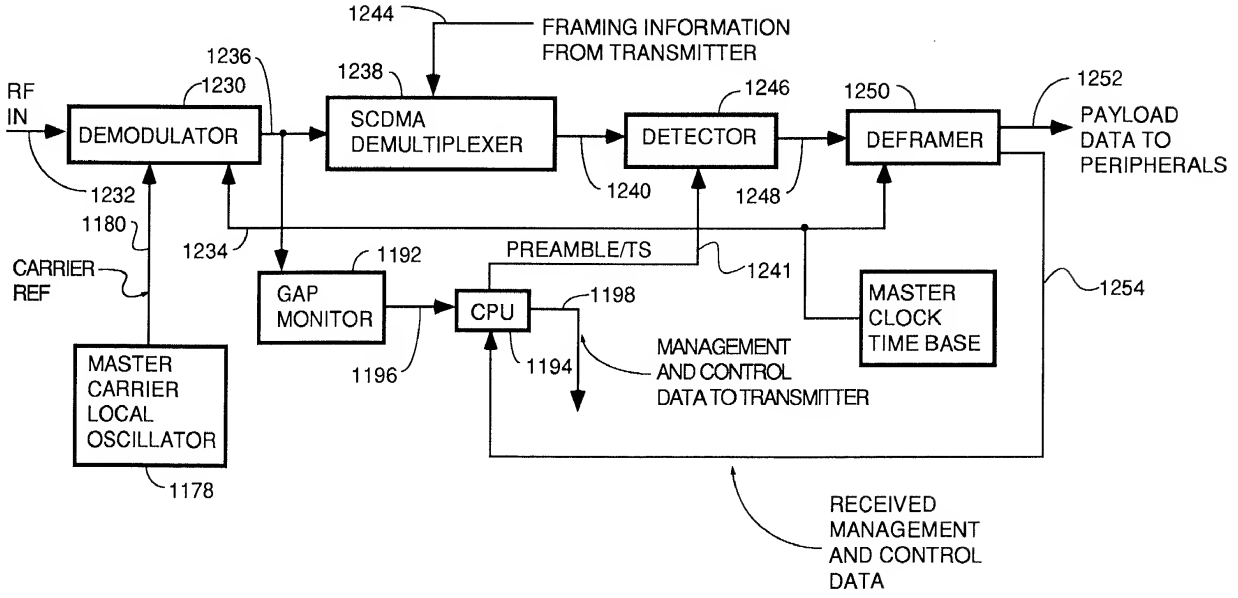
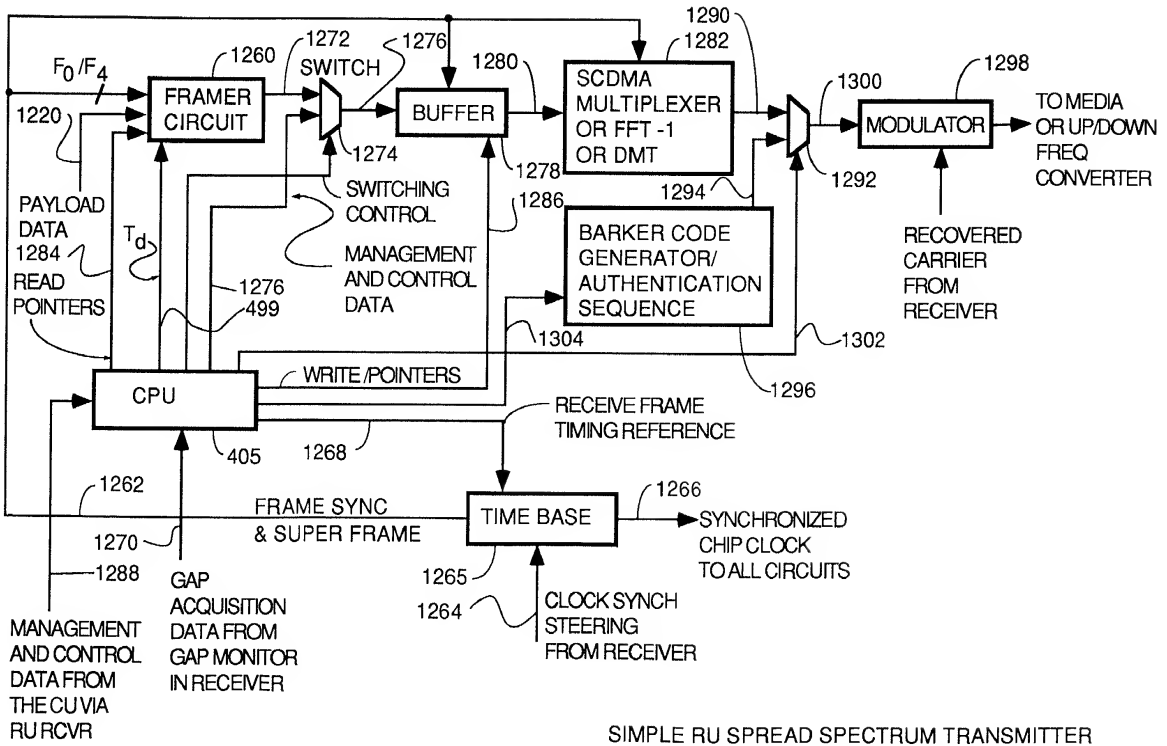

1166
BASEBAND DATA
1170
FRAMING/ ADDRESSING/ PACKETIZATION CIRCUIT
ANY TDMA, FDMA, STDMA, CDMA, INVERSE FOURIER, SCDMA OR DMT TRANSMITTER
RF
UP/DOWN FREQ. CONVERTER
1174
1168
PAYLOAD DATA IN
1200
MASTER CARRIER
PERIPHERALS/ PHONE NETWORK/ INTERNET/ SATELLITE/ CELLULAR INTERFACES
MASTER CLOCK
1176
CARRIER MASTER LOCAL OSCILLATOR
1178
1198
MASTER CLOCK
1194
CPU
PREAMBLE DATA
1181
1195
1196
1192
1180
GAP MONITOR
1254
1172
PAYLOAD DATA OUT
SCDMA RECEIVER
UPSTREAM RF
1252
1160
CU MODEM
DOWN-STREAM RF
HFC OR WIRELESS TRANSMISSION MEDIA
DOWN-STREAM RF
1190
TDMA, STDMA, FDMA, INVERSE FOURIER, SCDMA,CDMA OR DMT RECEIVER
1216
1162
UPSTREAM RF
RECOVERED MASTER CLOCK
1202
RECOVERED CARRIER
1226
1228
1214
PAYLOAD DATA OUT
UP/DOWN FREQ. CONVERTER
PERIPHERALS ETC.
1204
M &C AND GAP ACQ DATA
1218
1224
CPU
1208
T_d
1212
1216
1210
RF
PAYLOAD DATA IN
RANGING GEN
SEDMA RU TRANSMITTER
1220
1206
1164
RU MODEM

FIG. 54



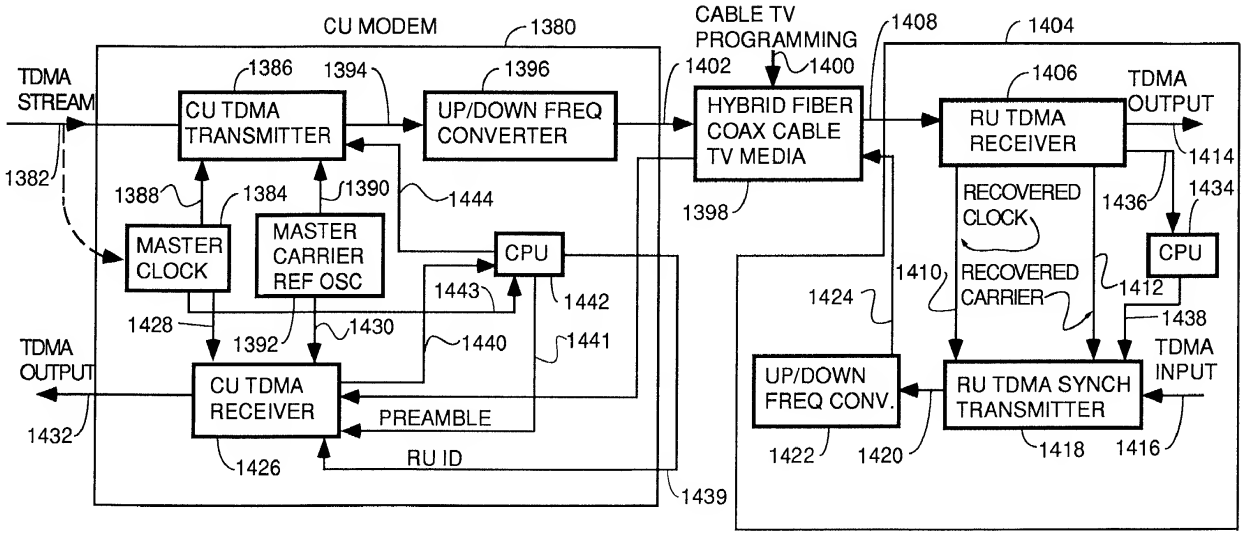
SIMPLE CU SPREAD SPECTRUM RECEIVER

FIG. 55



SIMPLE RU SPREAD SPECTRUM TRANSMITTER

FIG. 56



SYNCHRONOUS TDMA SYSTEM

FIG. 57

OFFSET	1B ASIC		2A ASIC	
(CHIPS)	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

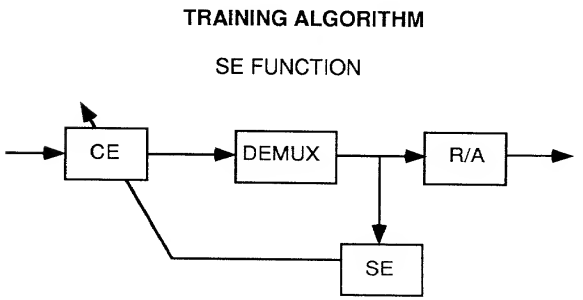
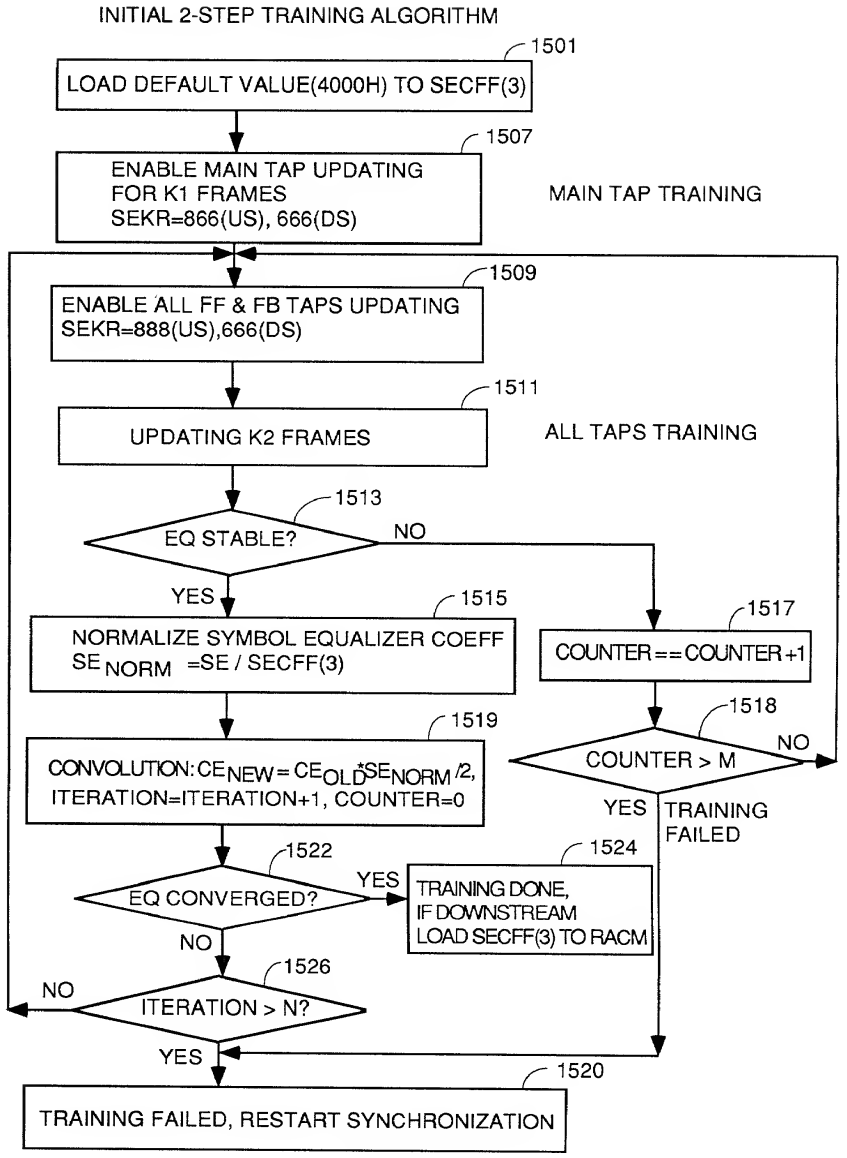


FIG. 59



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

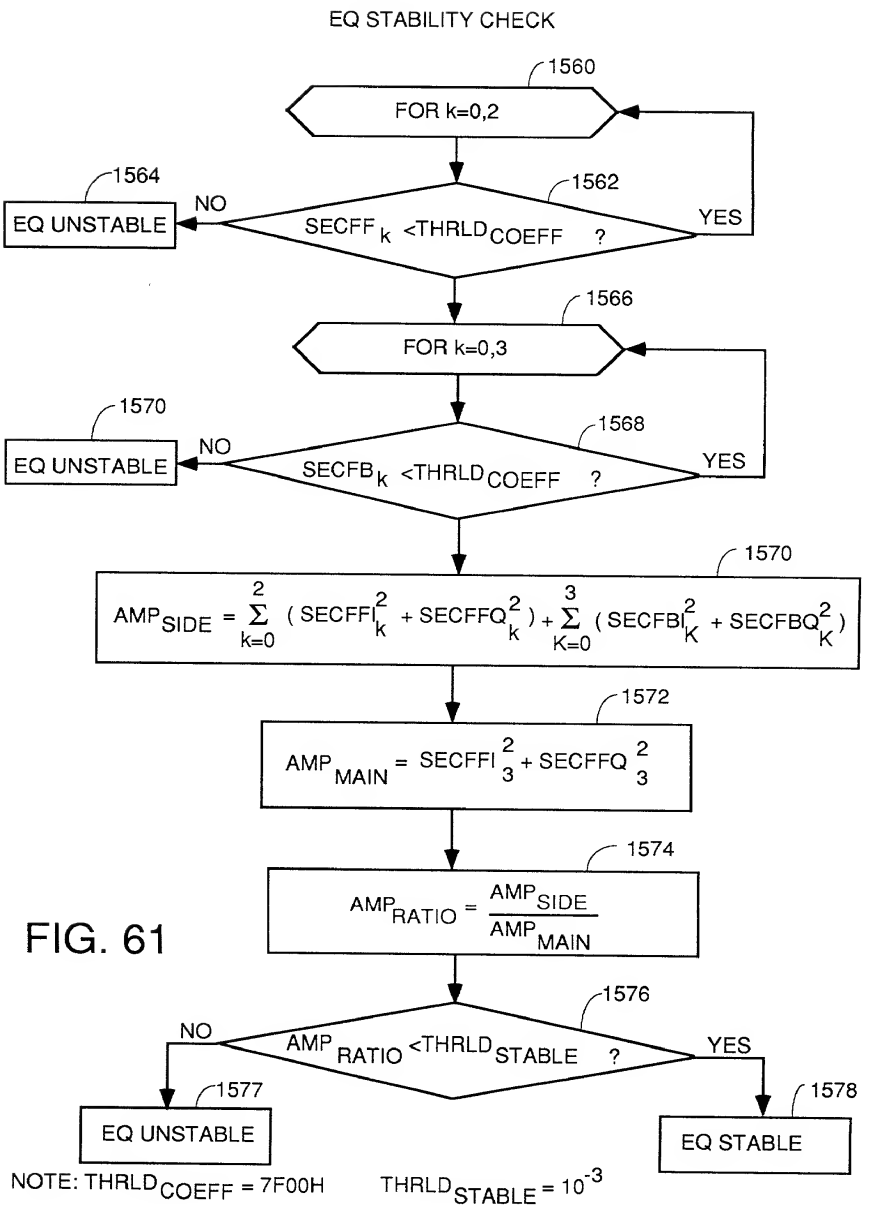
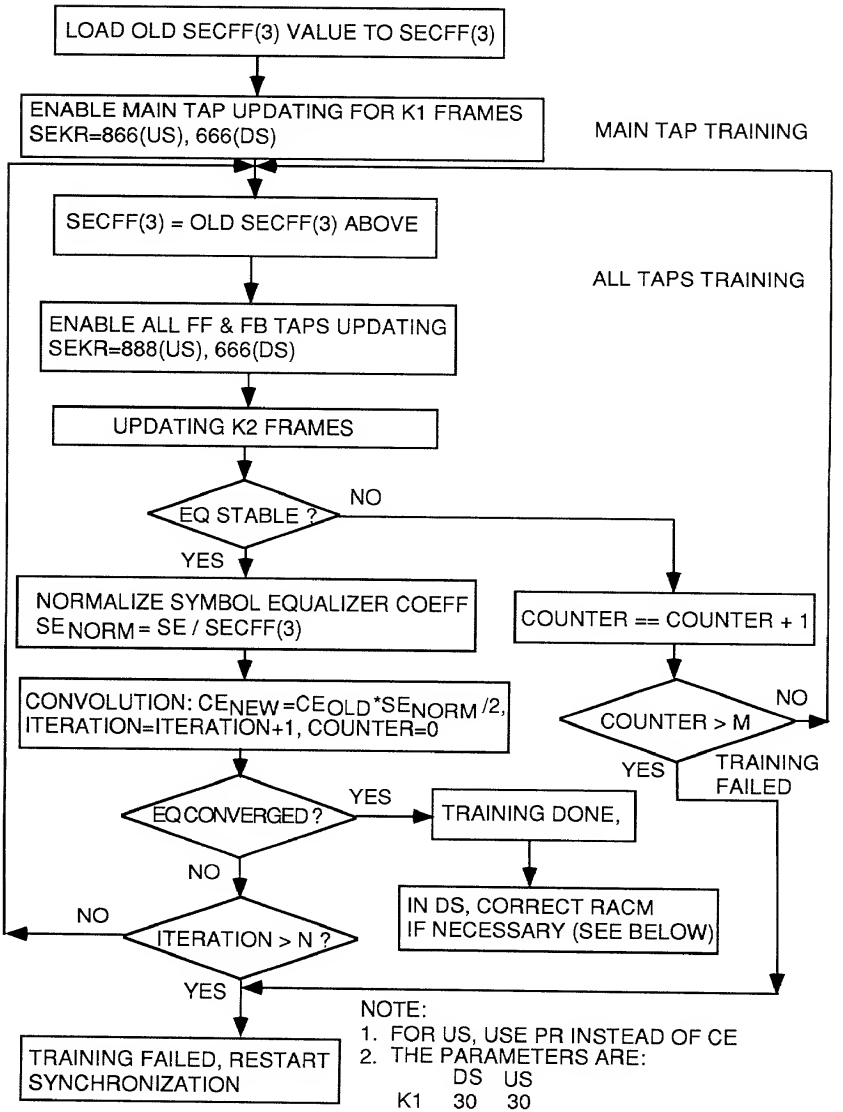

EQ STABILITY CHECK
1560
FOR k=0,2
1562
SECFF k <THRLD COEFF ?
NO
YES
1564
EQ UNSTABLE
1566
FOR k=0,3
1568
SECFB k <THRLD COEFF ?
NO
YES
1570
EQ UNSTABLE
1570
AMP SIDE = Σ (SECFFI k 2 + SECFFQ k 2) + Σ (SECFBI K 2 + SECFBQ K 2)
1572
AMP MAIN = SECFFI 3 2 + SECFFQ 3 2
1574
AMP RATIO = AMP SIDE / AMP MAIN
1576
AMP RATIO <THRLD STABLE ?
NO
YES
1577
EQ UNSTABLE
1578
EQ STABLE
NOTE: THRLD COEFF = 7F00H
THRLD STABLE = 10-3

FIG. 61

PERIODIC 2-STEP TRAINING ALGORITHM

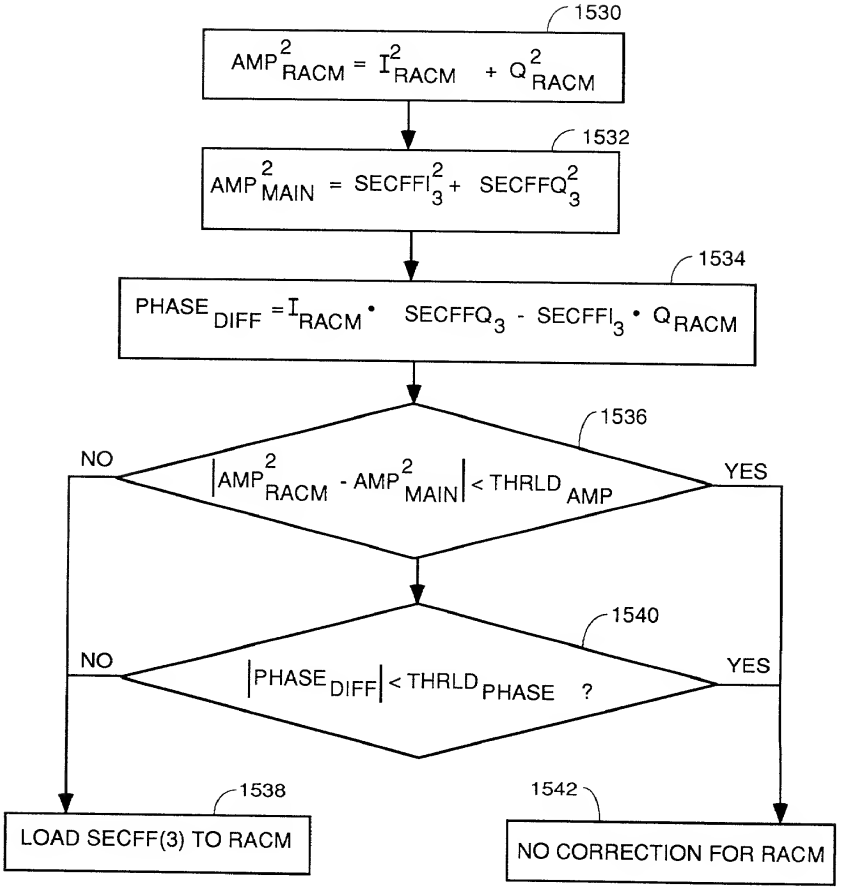


NOTE:
1. FOR US, USE PR INSTEAD OF CE
2. THE PARAMETERS ARE:

	DS	US
K1	30	30
K2	20	30
N	5	3
M	3	3

FIG. 62

RACM CORRECTION



NOTE: $THRLD_{AMP}$ = TBD

$THRLD_{PHASE}$ = TBD

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63

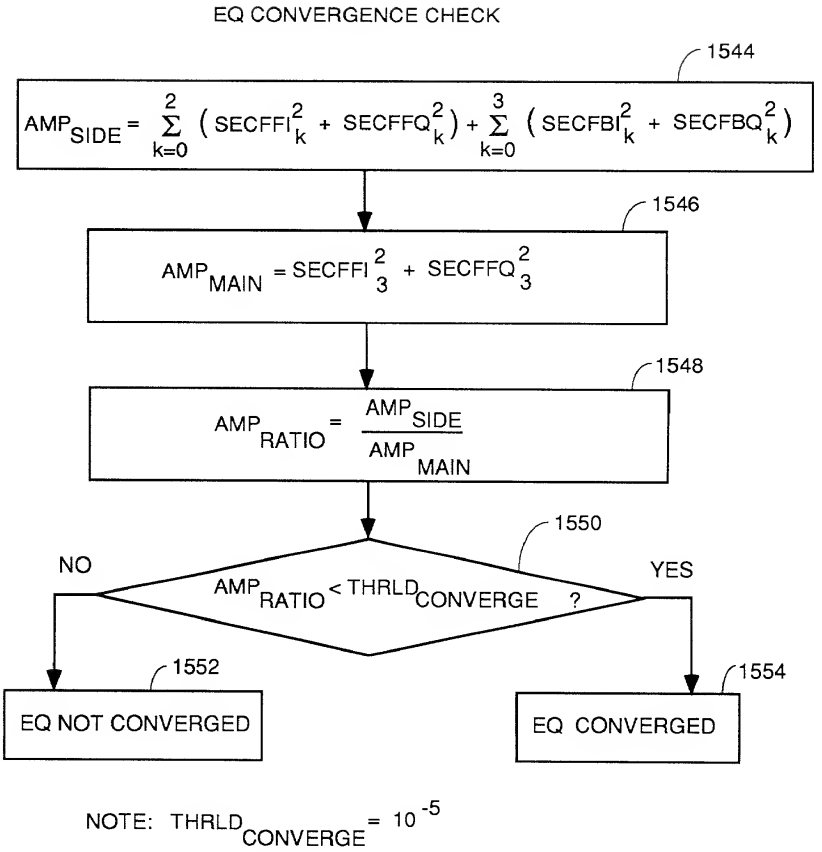

EQ CONVERGENCE CHECK
1544
$AMP_{SIDE} = \sum_{k=0}^{2} (SECFFI_k^2 + SECFFQ_k^2) + \sum_{k=0}^{3} (SECFBI_k^2 + SECFBQ_k^2)$
1546
$AMP_{MAIN} = SECFFI_3^2 + SECFFQ_3^2$
1548
$AMP_{RATIO} = \frac{AMP_{SIDE}}{AMP_{MAIN}}$
1550
$AMP_{RATIO} < THRLD_{CONVERGE}$?
NO
YES
1552
EQ NOT CONVERGED
1554
EQ CONVERGED
NOTE: $THRLD_{CONVERGE} = 10^{-5}$

FIG. 64

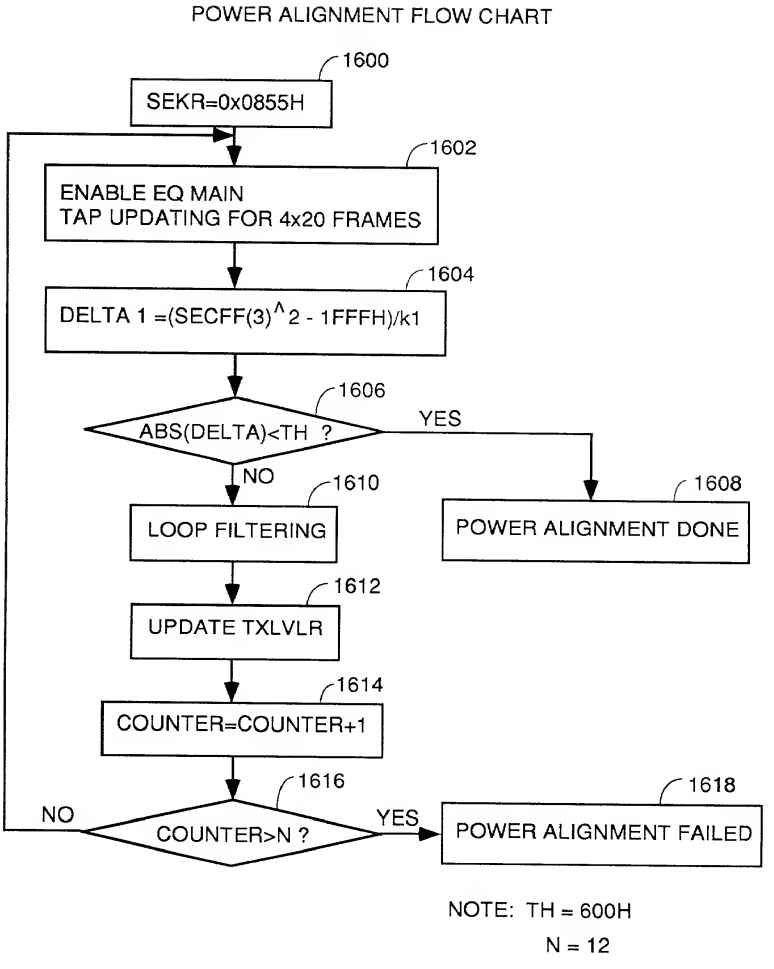

POWER ALIGNMENT FLOW CHART
1600
SEKR=0x0855H
1602
ENABLE EQ MAIN
TAP UPDATING FOR 4x20 FRAMES
1604
DELTA 1 =(SECFF(3)^2 - 1FFFH)/k1
1606
ABS(DELTA)<TH ?
YES
NO
1608
POWER ALIGNMENT DONE
1610
LOOP FILTERING
1612
UPDATE TXLVLR
1614
COUNTER=COUNTER+1
1616
NO
COUNTER>N ?
YES
1618
POWER ALIGNMENT FAILED
NOTE: TH = 600H
N = 12

FIG. 65

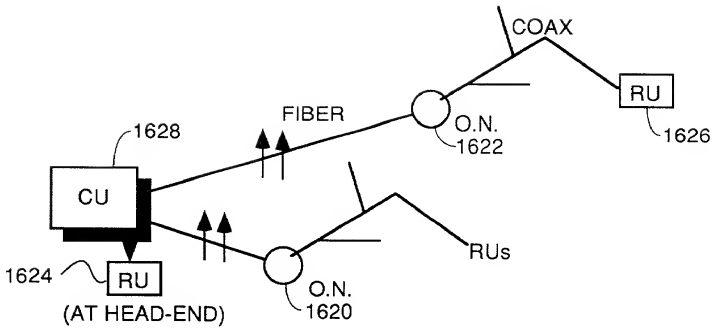
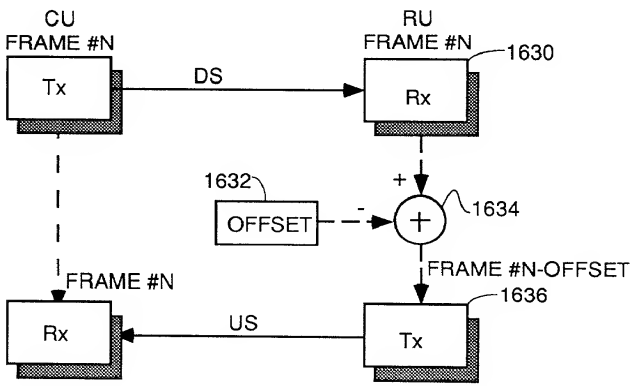


FIG. 66



TOTAL TURN AROUND (TTA) IN FRAMES = OFFSET

FIG. 67

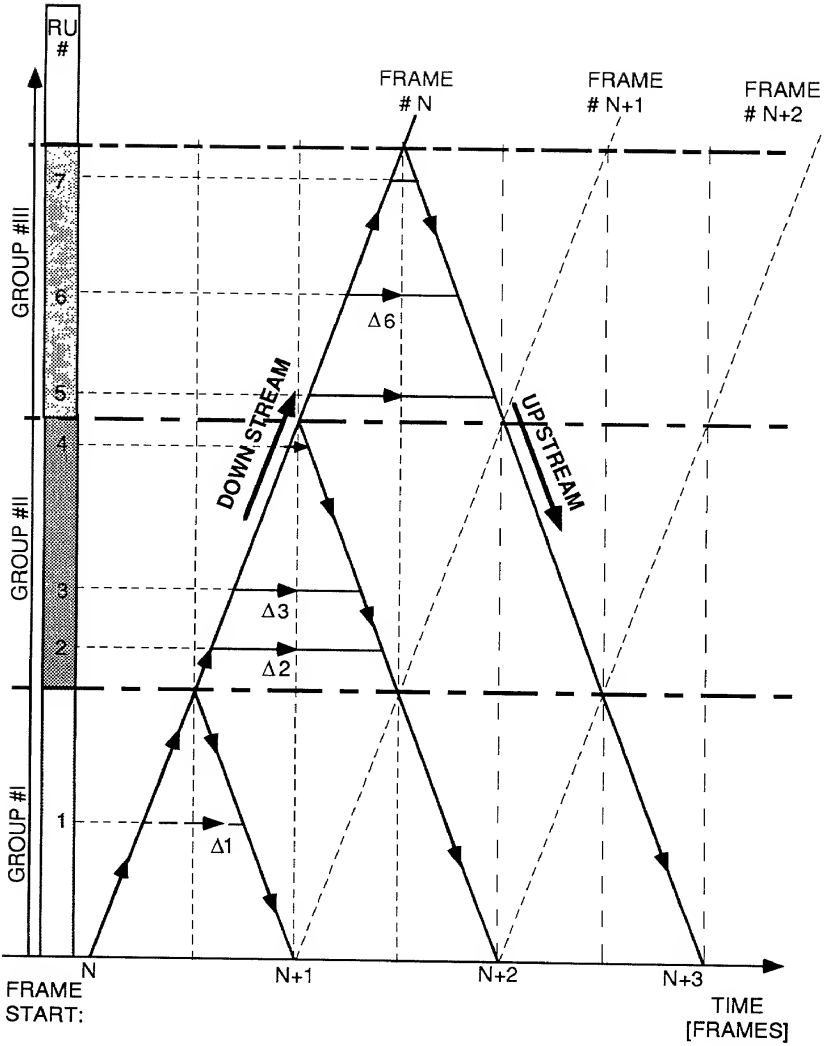
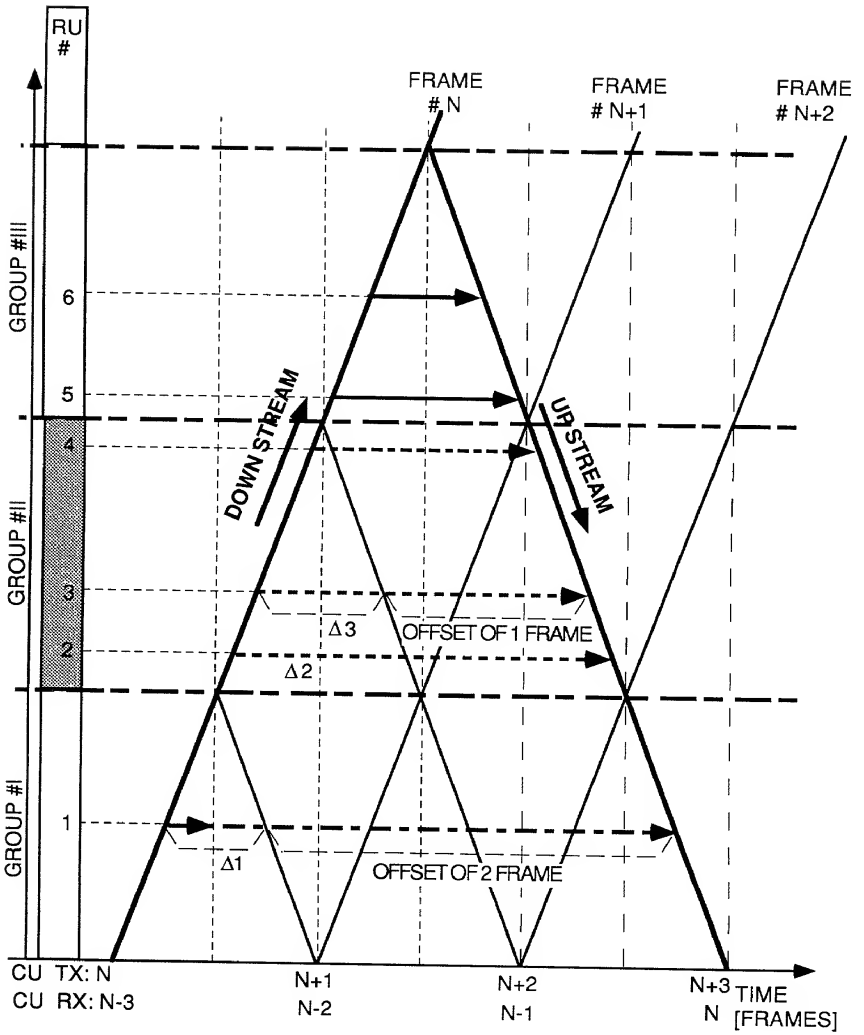

RU #
FRAME # N
FRAME # N+1
FRAME # N+2
GROUP #III
GROUP #II
GROUP #I
7
6
5
4
3
2
1
Δ6
Δ3
Δ2
Δ1
DOWN STREAM
UPSTREAM
N
N+1
N+2
N+3
FRAME START:
TIME [FRAMES]

FIG. 68



CONTROL MESSAGE (DOWNSTREAM) AND FUNCTION (UPSTREAM) PROPAGATION IN A 3 FRAMES TTA CHANNEL

FIG. 69

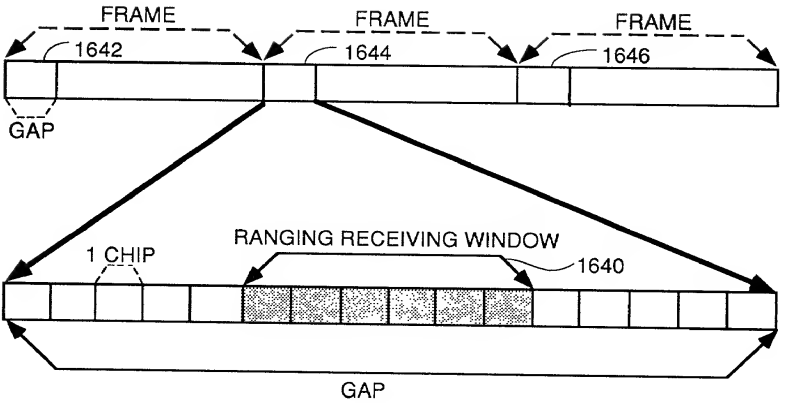
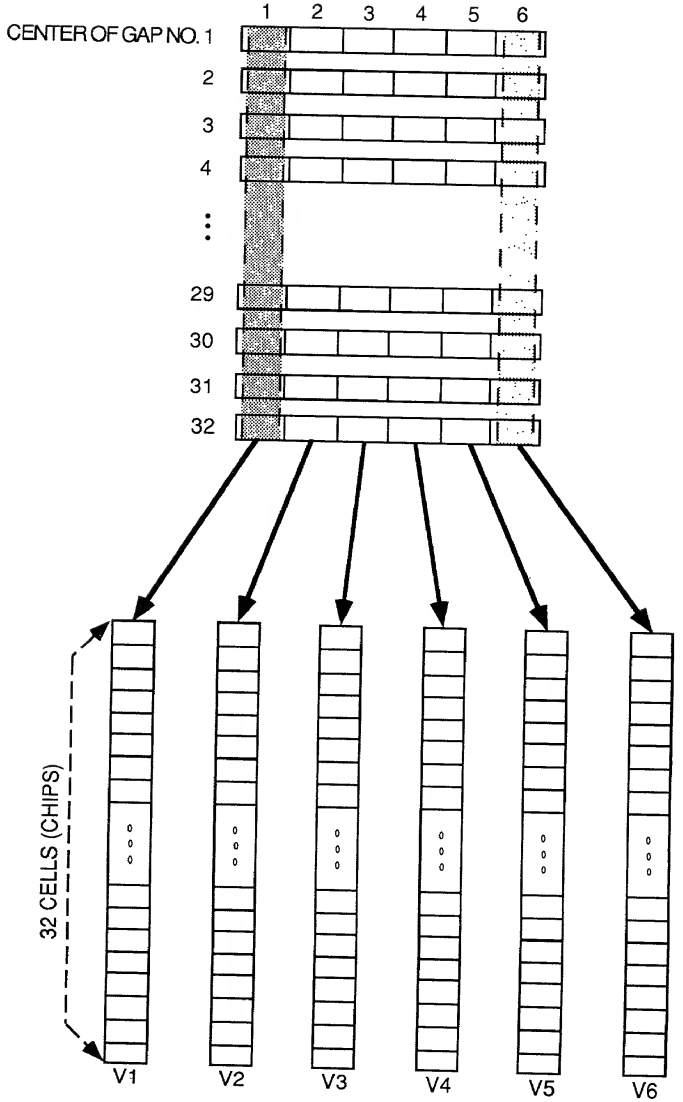

FRAME
FRAME
FRAME
1642
1644
1646
GAP
1 CHIP
RANGING RECEIVING WINDOW
1640
GAP

FIG. 70



OVERALL VIEW OF THE CU SENSING WINDOWS
IN A "BOUNDLESS RANGING" ALGORITHM

FIG. 71

CHIP\FR	1	2	3	4	5	6	7		33
1	0	0	1	0	0	1	1	•••	0
2	1	0	0	1	1	1	1	•••	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	•••	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	•••	

FIG. 72